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London WC2A 3LS (GB)(54) **A signal amplifier circuit and an image display device adopting the signal amplifier circuit.**

(57) A signal amplifier circuit is provided with a buffer amplifier (1) and an adjusting circuit (2) for detecting a difference in voltage between a reference voltage (V_0) and an output voltage ($V_0 + \Delta V$) of the buffer amplifier when the reference voltage (V_0) is inputted to the buffer amplifier (1) as an offset voltage, and for inputting a voltage obtained by subtracting the offset voltage (ΔV) from the voltage of an input signal so as to cancel out the offset voltage. An image display device of the present invention in-

cludes the above signal amplifier circuit. According to the above arrangement, the offset voltage (ΔV) can be cancelled out. Therefore, the signal amplifier circuit having a desirable buffer characteristic that a voltage having the same level as the voltage of the input signal can be outputted even if the offset voltage is generated in the buffer amplifier. By adopting the above signal amplifier circuit, an image display device which permits a high quality image display can be achieved.

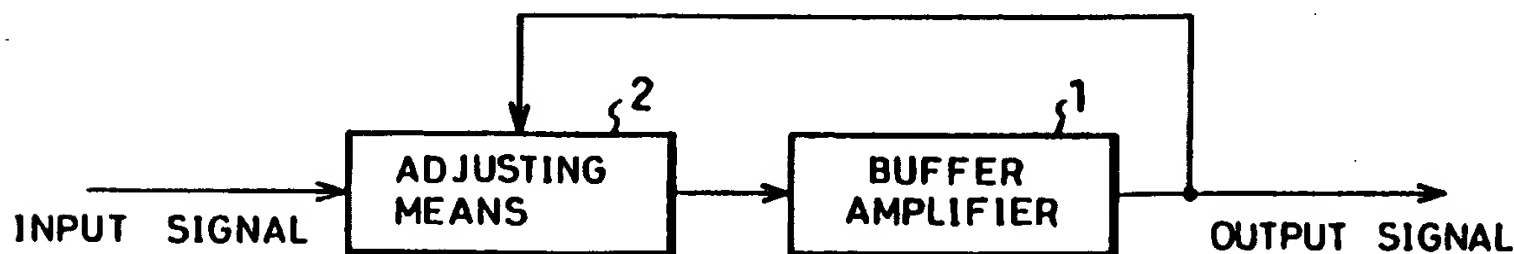
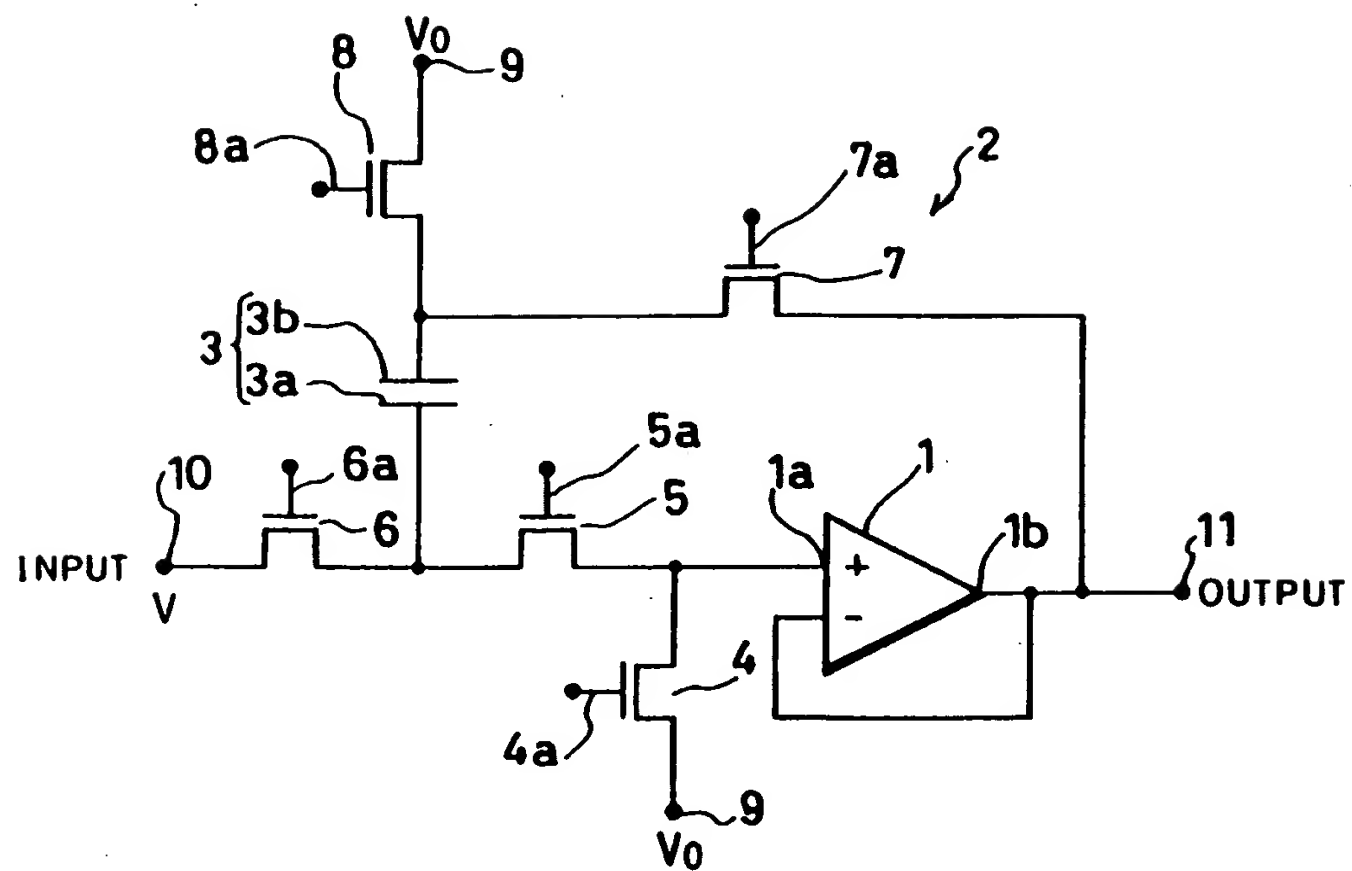
FIG. 1**EP 0 657 863 A2**

FIG. 2



FIELD OF THE INVENTION

The present invention relates to a signal amplifier circuit and an image display device such as a liquid crystal display, etc., adopting the signal amplifier circuit.

BACKGROUND OF THE INVENTION

A buffer amplifier has characteristics of high input impedance and low output impedance and of a voltage gain of substantially 1. Having the above characteristics, the buffer amplifier is used in a variety of fields.

The following descriptions will discuss the buffer amplifier through an example of an image display device of an active-matrix drive system provided with the buffer amplifier.

As shown in Fig. 12, the image display device of the active-matrix drive system is composed of drive circuits 101 and 102 and a display 103.

The display 103 is composed of display cells C_{ij} arranged so as to form a matrix. The drive circuit 101 samples a video signal so as to send an obtained voltage by sampling as data over a data signal line S_j . The drive circuit 102 selects a scanning signal line G_i in order so as to send data on the data signal line S_j to a display cell C_{ij} .

As shown in Fig. 13, in the case of liquid crystal displays, each display cell C_{ij} is composed of a liquid crystal element 104 and a FET 105 (field effect transistor) for driving the liquid crystal element 104. Additionally, a condenser 106 may be provided in the display cell C_{ij} if necessary.

A gate of the FET 105 is connected to the scanning signal line G_i , and a drain and a source of the FET 105 are respectively connected to the data signal line S_j and an electrode of the liquid crystal element 104. The other electrode of the liquid crystal element 104 is connected to a line used in common for all the display cells C_{ij} . As a result, a transmittance or a reflectance of a liquid crystal of the liquid crystal element 104 are adjusted based on data. In the described manner, an image corresponding to a video signal is displayed on the display 103 composed of display cells C_{ij} .

A drive circuit 101 is classified into two kinds: a digital driver for outputting digital data to the data signal line S_j ; and an analog driver for outputting analog data to the data signal line S_j .

As an example of digital drivers, a digital driver for a 3 bits-input, i.e., an 8 gradation ($= 2^3$) display is shown in Fig. 14.

The digital driver is composed of a shift register 107, a plurality of latches 108, a plurality of switching circuits 109 and a plurality of digital buffers 110.

As shown in Fig. 15, the digital buffer 110 is composed of a decoder 111 for decoding a signal from the switching circuit 109 and a switching circuit 112 which makes a selection among voltage values of V_1 through V_8 in order to achieve the 8 gradation display according to an output from the decoder 111.

As described, in the case of digital drivers, voltage levels and switching circuits 112 are respectively required in the same number as the number of gradations. Therefore, in the case of the multiple gradation display, the circuit becomes larger in size. For this reason, the following analog driver is more suitable for the multiple gradation display.

The drive system for analog drivers is classified into the following two systems: dot sequential drive system and line sequential drive system.

As shown in Fig. 16, an analog driver of the dot sequential drive system is composed of a shift register 107, a plurality of latches 108 and a plurality of switching circuits 112. The analog driver outputs data over the data signal line S_j by opening and closing the switching circuits 112 in synchronous with a pulse from each block of the shift register 107.

A period in which an output of data over the data signal line S_j is permitted is H_1/N where H_1 indicates an effective horizontal scanning period (approximately 80 % of the horizontal scanning period) and N indicates a number of picture elements in a horizontal direction, i.e., a number of display cells C_{i1} to C_{iN} . For this reason, in the case of displaying on a large screen, a period for outputting data over the data signal line S_j becomes short.

As shown in Fig. 17, an analog driver of the line sequential drive system is composed of a shift driver 107, a plurality of latches 108, a plurality of switching circuits 113, a plurality of condensers 116, a plurality of switching circuits 114, a plurality of condensers 117 and a plurality of buffer amplifiers 115 having the previously described characteristics.

Various kinds of circuits are applicable to the buffer amplifier 115 as shown in Fig. 18 through Fig. 20.

In the line sequential drive system, data from the switching circuit 113 is temporarily held in a sampling-use condenser 116 of a small capacity, and the switching circuits 114 are turned ON by a transfer signal in the next horizontal blanking period. As a result, all the data sent in the previous horizontal scanning period are sent to the respective holding condensers 117 and the buffer amplifiers 115 at one time, and are outputted to the data signal line S_j . Therefore, a sufficient length of the period for outputting data over the data signal line

S_j can be ensured.

In the described liquid crystal display device of the active-matrix drive system, the FET 105 of the display cell C_{ij} (see Fig. 13) is formed using a thin film made of amorphous silicon formed on a transparent substrate, and drive circuits 101 and 102 are manufactured as separately provided ICs (integrated circuits). Recently, a monolithic system technology has been reported for forming the drive circuits 101 and 102 and the display 103 on a thin film made of polycrystalline silicon.

However, in the case of a transistor composed of the thin film made of polycrystalline silicon, since a particle diameter and a channel length of the transistor have the same order, properties such as a threshold voltage, mutual conductance, sub-threshold coefficient, etc., differ for each transistor. Thus, in the case of manufacturing the buffer amplifier 115 (see Fig. 18 through Fig. 20), by the transistor made of the thin film made of polycrystalline silicon, the problem is presented in that an offset voltage is generated in the buffer amplifier 115. Here, the offset voltage is defined as a difference in voltage between the input voltage and the output voltage of the buffer amplifier 115.

The offset voltage differs for each buffer-amplifier 115, and this difference in the offset voltage may exceed 1 V. In the case of the liquid crystal display having a drive voltage (dynamic range) of 5 V, if a difference of offset voltages among buffer amplifiers 115 exceeds 1 V, a multiple gradation display of above 4 gradations cannot be carried out.

In order to counteract the above problem, the Japanese Laid-Open Patent Publication No. 1425941/1992 (Tokukaihei 4-142591) discloses a liquid crystal display device wherein a voltage for cancelling out the offset voltage is stored beforehand in the memory as adjusting data, and after adding the adjusting data to a video signal, the video signal is inputted into the drive circuit 101, thereby cancelling out the offset voltage.

However, when adopting the above liquid crystal display device, the following problems are newly raised: since a memory is required, a manufacturing cost goes up; and it takes time because an offset voltage is measured beforehand for each buffer amplifier 115 before being stored in the memory.

Moreover, since a Fermi level and a carrier mobility of a semiconductor has high temperature dependency, depending of an environmental temperature at which the liquid crystal display device is operated, the offset voltage may not be cancelled out. Furthermore, when using the transistor composed of the thin film made of polycrystalline silicon, the above properties greatly change as time passes because of the reasons that many

localized levels exist on a crystal grain boundary and a gate dielectric film - polycrystalline silicon interface, and the polycrystalline silicon thin film is in a state of floating potential, thereby presenting the problem that cancelling out of the offset voltage cannot be ensured for a long period of time.

As described, the following problems still remain unsolved: the offset voltage generated in the buffer amplifier 115, especially, when the buffer amplifier 115 is manufactured using the transistor composed of the polycrystalline silicon thin film, a large offset voltage generated.

Furthermore, when adopting the buffer amplifiers 115 in which offset voltage generates, since the offset voltage differs for each buffer amplifier 115, a high quality image display cannot be achieved.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a signal amplifier circuit having a desirable buffer characteristic that a signal inputted thereto has the same voltage level as a signal outputted therefrom with a simple structure.

In order to achieve the above object, a signal amplifier circuit of the present invention is characterized by comprising:

a buffer amplifier; and

adjusting means for detecting a difference in voltage as an offset voltage between a reference voltage and an output voltage from the buffer amplifier when the reference voltage is inputted thereto, and for inputting a voltage obtained by subtracting the offset voltage from a voltage of an input signal into said buffer amplifier so as to cancel out the offset voltage.

According to the above arrangement, since the offset voltage can be cancelled out, even if the offset voltage generates in the buffer amplifier, a signal amplifier circuit having a desirable buffer characteristic that the signal inputted thereto has the same voltage level as the signal outputted therefrom can be achieved.

Another object of the present invention is to provide an image display device which enables a high quality image display.

In order to achieve the above object, an image display device of the present invention which comprises:

a buffer amplifier;

a display composed of display cells arranged so as to form a matrix;

a first drive circuit for sampling a video signal so as to send a voltage obtained by sampling as data over a data signal line; and

a second drive circuit for selecting a scanning signal line in order so as to send data on the data signal line to each display cell,

wherein the first drive circuit includes:
 a shift register;
 switching circuits in the same number as the
 number of display cells in a lateral direction;
 sampling-use condensers in the same number as
 the number of the switching circuits; and
 signal amplifier circuits in the same number as
 the number of the sampling-use condensers,
 the shift register sends a signal in order into
 each switching circuit in synchronous with a clock
 signal,
 the switching circuit is then set ON when re-
 ceiving a signal from the shift register,
 each condenser samples a level of a video
 signal obtained when the switching circuit is set
 ON as data,
 when data in the same number as the number
 of the display cells in a lateral direction are held in
 the sampling-use condensers, the signal amplifier
 circuits take-in the data from the condensers at one
 time and output the data over the data signal line,
 thereby displaying the video signal to the display,
 the image display device is characterized in that
 the signal amplifier circuit includes:
 a buffer amplifier; and
 adjusting means for detecting a difference in
 voltage as an offset voltage between a reference
 voltage and an output voltage from the buffer am-
 plifier when the reference voltage is inputted there-
 to, and for inputting a voltage obtained by subtrac-
 ting the offset voltage from a voltage of a video
 signal sampled by each condenser into the buffer
 amplifier so as to cancel out the offset voltage.

According to the above arrangement, a voltage
 having the same level as a voltage temporarily held
 in the sampling-use condenser can be sent over
 the data signal line. As a result, a high quality
 image display is enabled.

For a fuller understanding of the nature and
 advantages of the invention, reference should be
 made to the ensuing detailed description taken in
 conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 through Fig. 11 and Fig. 21 show one
 embodiment of the present invention.

Fig. 1 is a view showing a schematic structure
 of a signal amplifier circuit in accordance with the
 present invention.

Fig. 2 is a circuit diagram showing the first
 example of the signal amplifier circuit of Fig. 1.

Fig. 3 is a timing chart of a control signal in the
 signal amplifier circuit of Fig. 2.

Fig. 4 is a circuit diagram which shows a
 sample configuration of a signal amplifier circuit
 which permits a shorter adjusting time.

Fig. 5 is a circuit diagram which shows another
 sample configuration of a signal amplifier circuit
 which permits a shorter adjusting time.

Fig. 6 is a circuit diagram which shows the
 second example of the signal amplifier circuit of
 Fig. 1.

Fig. 7 is a timing chart of a control signal in the
 signal amplifier circuit of Fig. 6.

Fig. 8 is a circuit diagram which shows the
 third example of the signal amplifier circuit of Fig.
 1.

Fig. 9 is a timing chart of a control signal in the
 signal amplifier circuit of Fig. 8.

Fig. 10 is a block diagram which shows a
 schematic configuration of a liquid crystal display
 device as an application example of the signal
 amplifier circuit of Fig. 1.

Fig. 11 is a block diagram showing a sche-
 matic configuration of a drive circuit for sending
 data over a data signal line in the liquid crystal
 display device of Fig. 10.

Fig. 21 is a timing chart showing an operation
 of the drive circuit of Fig. 11.

Fig. 12 through Fig. 20 show prior art.

Fig. 12 is a block diagram showing a sche-
 matic configuration of a conventional image display
 device of an active-matrix drive system.

Fig. 13 is a circuit diagram showing a configu-
 ration of a display cell in the case where the image
 display device of Fig. 12 is a liquid crystal display
 device.

Fig. 14 is a block diagram showing a sche-
 matic configuration of a digital driver as an exam-
 ple of the drive circuit for sending data in the data
 signal line over the image display device of Fig. 12.

Fig. 15 is a block diagram showing a sche-
 matic configuration of a digital buffer in the digital
 driver of Fig. 14.

Fig. 16 is a block diagram showing a sche-
 matic configuration of an analog driver of a dot
 sequential drive system as another example of the
 drive circuit for sending data over the data signal
 line in the image display device of Fig. 12.

Fig. 17 is a block diagram showing a sche-
 matic configuration of an analog driver of a line
 sequential drive system as still another example of
 the drive circuit for sending data over the data
 signal line in the image display device of Fig. 12.

Fig. 18 is a circuit diagram shown an example
 of the buffer amplifier in the analog driver of Fig.
 17.

Fig. 19 is a circuit diagram showing another
 example of the buffer amplifier in the analog driver
 of Fig. 17.

Fig. 20 is a circuit diagram showing still an-
 other example of the buffer amplifier in the analog
 driver of Fig. 17.

DESCRIPTION OF THE EMBODIMENTS

The following description will discuss embodiments of the present invention with reference to Fig. 1 through Fig. 11 and Fig. 21.

As shown in Fig. 1, a signal amplifier circuit in accordance with the present embodiment is provided with a buffer amplifier 1 and adjusting means 2 for cancelling out an offset voltage ΔV generated in the buffer amplifier 1.

The adjusting means 2 inputs a reference voltage V_0 to the buffer amplifier 1 and detects a difference between an output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 and a reference voltage V_0 as an offset voltage ΔV . Then, the adjusting means 2 inputs a voltage ($V - \Delta V$) obtained by subtracting the offset voltage ΔV from the voltage V of the input signal into the buffer amplifier 1.

When the voltage ($V - \Delta V$) is inputted to the buffer amplifier 1, a voltage ($V - \Delta V + \Delta V$) is outputted. Namely, the offset voltage ΔV is cancelled out, and the voltage V is outputted. According to the signal amplifier circuit of the present embodiment, even if the offset voltage ΔV is generated in the buffer amplifier 1, a desirable buffer characteristic that a signal outputted therefrom has the same voltage level as a signal inputted thereto can be achieved.

Therefore, even when the buffer amplifier 1 is manufactured using a transistor composed of a polycrystalline semiconductor or amorphous semiconductor, a signal amplifier circuit having a desirable buffer characteristic can be achieved.

It may be arranged such that the adjusting means 2 detects the offset voltage ΔV when the signal amplifier circuit starts operating. However, in the case where an input signal is inputted in synchronous with a clock signal, a detection of the offset voltage ΔV is preferably carried out at every clock.

In the above arrangement where the offset voltage ΔV is cancelled out at every clock, even if the offset voltage ΔV changes due to a change in the environment under which the signal amplifier circuit operates (for example, a change in temperature) or due to a change in properties of the signal amplifier circuit as time passes, cancelling out of the offset voltage ΔV can be always ensured.

The first example of the signal amplifier circuit will be explained below in reference to Fig. 2.

The signal amplifier circuit is composed of a buffer amplifier 1 and the adjusting means 2. The adjusting means 2 is composed of a condenser 3 (first condenser) and switching elements 4-8 (first - fifth switching elements).

An input terminal 1a of the buffer amplifier 1 is connected to an input terminal 9 of a reference voltage V_0 via the switching element 4. The input

terminal 1a of the buffer amplifier 1 is also connected to one electrode 3a of the condenser 3 via the switching element 5. The electrode 3a is connected to an input terminal 10 of the signal amplifier circuit via the switching element 6. The other electrode 3b of the condenser 3 is connected to an output terminal 1b of the buffer amplifier 1 via the switching element 7. The electrode 3b of the condenser 3 is also connected to an input terminal 9 via the switching element 8.

In order to stabilize a signal level, another condenser of a small capacity may be added to the input terminal 1a of the buffer amplifier 1. This is effective if respective parasitic capacities of the buffer amplifier 1 and switching elements 4 and 5 and the capacity of wires used in connecting the above components are not sufficient for stabilizing the signal level.

Hereinafter, it is assumed that the buffer amplifier 1 always generates a constant offset voltage ΔV as long as the level of an input signal falls within a predetermined range.

The switching elements 4-8 are respectively controlled by control signals 4a - 8a from the control means (not shown) according to a timing chart of Fig. 3.

It is shown in Fig. 3 that respective rises and falls of control signals 4a-8a completely coincide in a time period of $t_1 - t_5$. In practice, however, when respective levels of the control signals 4a-8a change, finite time (transition time) is required. Therefore, in order to cancel out an offset voltage ΔV accurately, it is necessary to prevent an interference by a transient signal generated at respective rises and falls of the control signals 4a-8a. For the reason above, it is preferably prevent an interference occurred at rises and falls of the control signals 4a-8a, for example, by delaying a rise of one of the control signals 4a-8a. Additionally, the control signals 4a-8a are applicable to the case where a N-channel MOS transistor is adopted as switching elements 4-8. However, when P-channel MOS transistor is adopted as switching elements 4-8, the phase of the control signals 4a-8a should be reversed. The above features are also true of a timing chart to be described later.

At t_1 , control signals 4a, 5a and 7a are High level and control signals 6a and 8a are Low level, and thus switching elements 4, 5 and 7 are set ON and switching elements 6 and 8 are set OFF.

Therefore, the reference voltage V_0 is applied to the input terminal 1a of the buffer amplifier 1 through a switching element 4; in the meantime, it is applied to the electrode 3a of the condenser 3 through the switching element 5. The output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 is applied to the electrode 3b of the condenser 3 through the switching element 7.

At t_2 , the control signal 5a is set to Low level, and the control signal 6a is set to High level. As a result, the switching element 5 is set OFF, and the switching element 6 is set ON.

For this reason, an input signal having a voltage V from the input terminal 10 is applied to the electrode 3a of the condenser 3 through the switching element 6.

At t_3 , the control signal 6a is set to Low level, and thus the switching element 6 is set OFF.

At t_4 , the control signal 7a is set to Low level, and the control signal 8a is set to High level. As a result, the switching element 7 is set OFF, and the switching element 8 is set ON.

Therefore, the reference voltage V_0 is applied to the electrode 3b of the condenser 3 through the switching element 8. As a result, a voltage of the electrode 3a of the condenser 3 becomes a voltage ($V - \Delta V$) obtained by shifting the voltage V of the input signal by a voltage changed in the electrode 3b (i.e., $V_0 - (V_0 + \Delta V) = -\Delta V$).

At t_5 , the control signal 4a is set to Low level, and the control signal 5a is set to High level. As a result, the switching element 4 is set OFF and the switching element 5 is set ON.

Thus, a voltage ($V - \Delta V$) of the electrode 3a of the condenser 3 is applied to the input terminal 1a of the buffer amplifier 1 through the switching element 5. As a result, the offset voltage ΔV is cancelled out, and the voltage V in the same level as the voltage V of the input signal is outputted from the output terminal 1.

In the described signal amplifier circuit, a time required for adjusting the offset voltage ΔV is ($t_5 - t_1$). However, by setting the load of the buffer amplifier smaller, the time required for adjusting the offset voltage ΔV can be made shorter. This is because in the adjusting period, a stabilization of the output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 when the reference voltage V_0 is inputted requires the longest time. Especially, when a difference between the input signal level and the reference voltage V_0 before adjusting the offset voltage ΔV is large, the stabilization requires a long time.

More specifically, it may be arranged such that a switching element 21 (eighth switching element) for applying a reference voltage V_0 to an output terminal 1b of the buffer amplifier in a period directly before t_1 is provided as shown in Fig. 4. Alternatively, it may be arranged such that a switching element 22 (ninth switching element) for switching off the load from the output terminal 1b of the buffer amplifier 1 in a period between t_1 and t_5 is provided as shown in Fig. 5.

For the buffer amplifier 1, a circuit shown in the explanation of prior arts (see Fig. 18 and Fig. 20) may be used. However, the present invention is not

limited to this. Other circuits having the buffer characteristic may be applicable.

The second example of the signal amplifier circuit will be explained below in reference to Fig. 6.

In the signal amplifier circuit, the switching element 4 of the first example is not provided. Instead, switching elements 14 and 15 (sixth and seventh switching elements) and a condenser 16 holding a reference voltage V_0 (second condenser) are additionally provided.

Switching elements 5-8, 14 and 15 are respectively controlled by control signals 5a - 8a, 14a and 15a from control means (not shown) according to a timing chart of Fig. 7.

At t_1 , the control signals 15a, 5a, 14a and 7a are High level, and control signals 6a and 8a are Low level. Thus, the switching elements 15, 5, 14 and 7 are set ON, and the switching elements 6 and 8 are set OFF.

For this reason, the reference voltage V_0 is applied to the condenser 16 through the switching elements 14, 5 and 15. As a result, the condenser 16 is charged, and the potential of the input terminal 1a of the buffer amplifier 1 becomes the reference voltage V_0 . The offset voltage ΔV is cancelled out using a voltage of the terminal on the buffer amplifier side of the condenser 16 (i.e., reference voltage V_0). Other than the above, the signal amplifier circuit of this example has approximately the same configuration as the signal amplifier circuit of the first example.

In the signal amplifier circuit of this example, a time required for adjusting the offset voltage ΔV is ($t_4 - t_1$) of Fig. 7.

The third example of the signal amplifier circuit will be explained below in reference to Fig. 8.

In the signal amplifier circuit of this example, the switching element 5 of the first example is not provided. Instead, a condenser 17 (third condenser) for holding an output voltage from the buffer amplifier 1 is additionally provided. The electrostatic capacity of the condenser 17 is set significantly larger than that of the condenser 3.

Switching elements 4 and 6-8 are respectively controlled by control signals 4a and 6a-8a from the control means (not shown) according to a timing chart of Fig. 9.

At t_1 , the control signals 4a and 7a are High level, and the control signals 6a and 8a are Low level. Thus, the switching elements 4 and 7 are set ON, and the switching elements 6 and 8 are set OFF.

For this reason, the reference voltage V_0 is applied to the input terminal 1a of the buffer amplifier 1 through the switching element 4. The output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 is applied to the condenser 17 through the switching

element 7. As a result, the condenser 17 is charged, and the potential of the electrode 3b of the condenser 3 becomes the output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 when the reference voltage V_0 is inputted. Then, the offset voltage ΔV is cancelled out using the voltage ($V_0 + \Delta V$) held in the condenser 17. Other than the above, the signal amplifier circuit of this example has the same configuration as the previous example.

In the signal amplifier circuit of this example, a time required for cancelling the offset voltage ΔV is ($t_3 - t_1$) shown in Fig. 9.

In the present embodiment, the reference voltage V_0 is not specified as long as it falls within a range where the linearity of the buffer amplifier 1 is ensured. However, it is preferably set to a mid-value of a range of the input signal level of the signal amplifier circuit. As a result, the non-linearity of the buffer amplifier 1 can be minimized, thereby achieving an accurate signal amplifier circuit. Moreover, because a change in the output from the buffer amplifier 1 in a period required for cancelling out the offset voltage V_0 can be suppressed evenly, the time required for it can be reduced. Furthermore, since current applied to the condensers 3, 16 and 17 or switching elements 4-8, 14, 15, 21 and 22 can be made smaller, a transient generated at respective rises and falls of the control signals 4a-8a can be suppressed.

A constant voltage V_1 to be applied to an electrode of the condenser 16 on the other side of the switching element 15 and a constant voltage V_2 to be applied to an electrode of the condenser 17 on the other side of the switching element 7 are not specified as long as they are constant. However, for the reasons above, the constant voltage V_1 and V_2 are preferably set to a mid-value of a range of the input signal level of the signal amplifier circuit.

In the above examples, respective internal capacities of switching elements 4, 5... and parasitic capacities of wires are preferably set significantly smaller than the electrostatic capacity of the condenser 3 in order to surely cancel out the offset voltage ΔV .

For example, for each switching element 4, 5 ..., N-channel or P-channel MOS (metal oxide semiconductor) transistor, or a complementary MOS (CMOS) transistor switch composed of a N-channel MOS and a P-channel MOS connected in parallel may be used.

The N-channel MOS transistor and the P-channel MOS transistor, respective waveforms of gate electrodes when opening and closing a switch have phases opposite to one another. Therefore, by adopting the CMOS transistor switch, a potential shift due to the parasitic capacity between the gate electrode and the source electrode can be elimi-

nated. For the above reason, a more accurate signal amplifier circuit can be achieved by adopting the CMOS transistor switch.

In the above preferred examples, the condensers 3, 16 and 17 are used for holding a voltage. However, the present invention is not limited to this. For example, other kinds of analog memory means or digital memory means of a plurality of bits may be used. For the analog memory means, a condenser provided between metal wiring layers or between the metal wiring layer and a semiconductor layer may be used. For the digital memory means, other than those having the same configurations as the analog memory means (condenser), a logic circuit such as a flip-flop may be used.

As an application example of the signal amplifier circuit, a liquid crystal display of an active-matrix drive system adopting the signal amplifier circuit will be explained below.

As shown in Fig. 10, the liquid display is composed of drive circuits 51 and 52 (first and second drive means), a display 53 composed of display cells arranged so as to form a matrix and a timing signal generating circuit 54 (i.e., a clock signal and control signals 5a, 6a, ...) provided for controlling the drive circuits 51 and 52. The timing signal generating circuit 54 may be formed on the substrate whereon the display 53 is formed or on a substrate separately provided.

The drive circuit 51 samples a video signal in synchronous with the timing signal and sends a voltage obtained by sampling as data over the data signal line S_j (Fig. 11). The drive circuit 52 selects a scanning signal line G_i in order (Fig. 12), and data on the data signal line S_j is sent to a display cell of the display 53.

As shown in Fig. 11, an analog driver of linear sequential drive system which serves as the drive circuit 51 is composed of a shift register 57, a plurality of latches 58, a plurality of switching circuits 59, a plurality of condensers 60 and a plurality of signal amplifier circuits 61. Here, it is possible to omit latches 58.

As shown in Fig. 21, the shift register 57 sends a signal over latches 58 in order in synchronous with a clock signal. Each latch 58 holds a signal from the shift register 57 and shifts a signal level if necessary. Each switching circuit 59 is set ON by a signal from the latch 58, and the level of a video signal at that time is sampled to the condenser 60 as data. In the described manner, data of an effective horizontal scanning period, i.e., data of the same number as the number of picture elements in a lateral direction are held in a plurality of condensers 60 respectively.

As described, the signal amplifier circuit 61 is provided with the buffer amplifier 1 and the adjusting means 2 for cancelling out an offset voltage ΔV

of the buffer amplifier 1. Additionally, in the case of a liquid crystal display, the adjusting means 2 also has a function for holding data. The data from respective condensers 60 are read in the signal amplifier circuit 61 using a control signal at one time within the horizontal blanking period. However, an adjustment of the offset voltage ΔV including the process for reading-in the data is carried out either only in the horizontal blanking period or both the horizontal blanking period and the period directly before the horizontal blanking period using the control signal. When the offset voltage ΔV is cancelled out both in the horizontal blanking period and the period directly before and after the horizontal blanking period, although a sufficient time for the adjustment can be ensured, a period for outputting the video signal over the data signal line S_j may be shortened. However, this would not be a problem because the linear sequential drive system offers a long writing time.

According to the signal amplifier circuit 61 of the present embodiment, even if the offset voltage ΔV generates in the buffer amplifier 1, a voltage V of the same level as the voltage V of an input signal can be sent over the data signal line S_j . As a result, a high quality image display can be ensured, thereby permitting a display 53 of a larger size.

In the above arrangement, an adjustment of an offset voltage ΔV is carried out in every horizontal blanking period. Therefore, even if the offset voltage ΔV deviates due to a change in the environment under which the liquid crystal display is operated (for example, a change in temperature), or a change in properties of the signal amplifier circuit 61 as time passes, the offset voltage ΔV can be always and surely cancelled out.

In the above liquid crystal display, a single shift register 57 has been used. However, the present invention is not limited to this. For example, n numbers of shift registers connected in parallel may be used. In this case, a sampling period will be n times of that using a single shift register 57. Namely, a sufficient sampling time can be ensured.

The drive circuits 51 and 52 and the display 53 may be formed on different substrates. However, by forming either one of the drive circuits 51 and 52 or both of the drive circuits 51 and 52 on the substrate whereon the display is formed, a liquid crystal display wherein the drive circuits 51 and 52 and the display 53 are integrated can be achieved.

A single crystal silicon thin film transistor or polycrystalline silicon thin film transistor has its carrier mobility ten times as high as the amorphous silicon thin film transistor, and thus it is suitable for the drive circuits 51 and 52. Therefore, the substrate is preferably arranged such that a single crystal silicon thin film or polycrystalline thin film is

formed on a transparent substrate. In the above thin film transistors, since the respective substrates are in the floating potential state, the substrates do not affect the threshold voltage. Therefore, in the transistor for transferring a video signal, the above feature is advantageous because it is not necessary to consider a drop in the potential of a signal due to a rise in the threshold voltage.

The liquid crystal display of the present embodiment permits a high quality image display. Therefore, it is suitable not only for displaying an analog data (a video signal having a successive level change) but also for displaying a video signal having a discrete level (digital data) corresponding to the multiple gradation (above 4 gradations).

In the above preferred embodiment, the liquid crystal display has been explained as an application example of the signal amplifier circuit. However, the use of the signal amplifier circuit of the present invention is widespread. For example, it is applicable to an image display device such as a CRT (cathode-ray tube) display, VF (vacuum fluorescent) display, plasma display, EL (electroluminescence) display, etc.

Furthermore, the use of the signal amplifier circuit of the present embodiment is not limited to the image display device. It is also applicable to various devices adopting a buffer amplifier. By replacing the buffer amplifier with the signal amplifier of the present embodiment, an excellent buffer characteristic can be achieved.

The signal amplifier circuits and image display devices adopting the signal amplifier circuit disclosed in the present embodiment are for example as listed below.

The first signal amplifier circuit is provided with a buffer amplifier 1 and adjusting means 2. The adjusting means 2 detects a difference in voltage between a reference voltage V_0 and an output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 obtained when inputting the reference voltage V_0 to the buffer amplifier 1. An obtained difference in voltage is defined as an offset voltage ΔV . The adjusting means 2 cancels out the offset voltage ΔV by inputting a voltage obtained by subtracting the offset voltage ΔV from the voltage of the input signal.

According to the above arrangement, since the offset voltage ΔV can be cancelled out, a signal amplifier circuit having a desirable buffer characteristic that a signal inputted thereto has the same voltage level as a signal outputted therefrom can be ensured even if the offset voltage ΔV generates in the buffer amplifier 1.

The second signal amplifier circuit having the structure of the first signal amplifier circuit is arranged such that an input signal is inputted in synchronous with a clock, and the offset voltage

ΔV is cancelled out by the adjusting means 2 at every clock.

According to the arrangement of the second amplifier circuit, the following effect can be achieved in addition to the effect attained from the first signal amplifier circuit. By cancelling out the offset voltage ΔV at every clock, even if the offset voltage ΔV changes due to a change in the environment under which the signal amplifier circuit is operated (for example, change in temperature) or due to a change in characteristic of the signal amplifier circuit as time passes, cancelling out of the offset voltage ΔV can be always ensured.

The third signal amplifier circuit having the structure of the second signal amplifier circuit is arranged such that the adjusting means 2 is composed of a condenser 3 and switching elements 4-8, and that an input terminal 1a of the buffer amplifier 1 is connected to an input terminal 9 of a reference voltage V_0 through the switching element 4 and is also connected to one electrode 3a of the condenser 3 through the switching element 5. The third signal amplifier circuit is further arranged such that the electrode 3a of the condenser 3 is connected to an input terminal 10 of the input signal through the switching element 6, and the other electrode 3b of the condenser 3 is connected to an output terminal 1b of the buffer amplifier 1 through the switching element 7 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 8.

The third signal amplifier circuit enables a reduced number of components in addition to the effect of the second signal amplifier circuit.

The fourth signal amplifier circuit having the structure of the second signal amplifier circuit, the adjusting means 2 is composed of condensers 3 and 16 and switching elements 5-8, 14 and 15, and the input terminal 1a of the buffer amplifier 1 is connected to the electrode 3a of the condenser 3 through the switching element 5 and is connected to a constant voltage terminal through the switching element 15 and the condenser 16. The fourth signal amplifier circuit is further arranged such that the electrode 3a of the condenser 3 is connected to the input terminal 10 of the input signal through the switching element 6 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 14, and that the other electrode 3b of the condenser 3 is connected to the output terminal 1b of the buffer amplifier 1 through the switching element 7 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 8.

The fourth signal amplifier circuit enables a reduced number of components in addition to the effect of the second signal amplifier circuit.

The fifth signal amplifier circuit having the structure of the second signal amplifier circuit is arranged such that the adjusting means 2 is composed of condensers 3 and 17 and switching elements 4, 6-8, and the input terminal 1a of the buffer amplifier 1 is connected to the input terminal 9 of the reference voltage V_0 through the switching element 4 and is connected to the electrode 3a of the condenser 3. The fifth signal amplifier circuit is further arranged such that the electrode 3a of the condenser 3 is connected to the input terminal 10 of the input signal through the switching element 6, and the other electrode 1b of the condenser 3 is connected to the other output terminal 1b of the buffer amplifier 1 through the switching element 7 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 8. The other electrode 3b of the condenser 3 is also connected to the constant voltage terminal through the condenser 17.

The fifth signal amplifier circuit enables a reduced number of components in addition to the effect of the second signal amplifier circuit.

The sixth signal amplifier circuit having the structure of the first, second, third, fourth or fifth signal amplifier circuit is arranged such that a switching element 21 is provided for applying the reference voltage V_0 to the output terminal 1b of the buffer amplifier 1.

The sixth signal amplifier circuit permits a load of the buffer amplifier 1 to be reduced in addition to the effect obtained from the effect of the first, second, third, fourth or fifth signal amplifier circuit. Therefore, a time required for cancelling out the offset voltage ΔV can be shortened.

The seventh signal amplifier circuit having the arrangement of the first, second, third, fourth or fifth signal amplifier circuit is arranged such that a switching element 22 for separating the buffer amplifier 1 from an external load is provided.

The seventh signal amplifier circuit permits a load of the buffer amplifier 1 to be reduced in addition to the effect of the first, second, third, fourth or fifth signal amplifier circuit. Therefore, a time required for cancelling out an offset voltage ΔV can be reduced.

The eighth signal amplifier circuit having the structure of the third signal amplifier circuit is arranged such that at least one of the switching elements 4-8 is a complementary MOS transistor switch.

The eighth signal amplifier circuit permits a higher accuracy compared with the signal amplifier circuit adopting a N-channel or P-channel MOS transistor switch, in addition to the effect of the third signal amplifier circuit.

The ninth signal amplifier circuit having the structure of the fourth signal amplifier circuit is

arranged such that at least one of the switching elements 5, 8, 14 and 15 is a complementary MOS transistor switch.

The ninth signal amplifier circuit permits the same effect as the eighth signal amplifier circuit.

The tenth signal amplifier circuit having the structure of the fifth signal amplifier circuit is arranged such that at least one of the switching elements 4 and 6-8 is a complementary MOS transistor switch.

The tenth signal amplifier circuit permits the same effect as the eighth signal amplifier circuit.

In order to achieve the above object, the first image display device of the present invention comprises a display 53 composed of display cells arranged so as to form a matrix; a drive circuit 51 for sampling a video signal so as to send a voltage obtained by sampling as data over a data signal line S_j ; and a drive circuit 52 for selecting a scanning signal line in order so as to send data on the data signal line S_j to a display cell, wherein the drive circuit 51 comprises a shift register 57; switching circuits 59 in the same number as the number of display cells in a lateral direction; sampling-use condensers 60 in the same number as the number of switching circuits 59 and signal amplifier circuits 61 in the same number of sampling-use condensers 60. The first image display device is arranged such that the shift register 57 sends a signal to the switching circuits 59 in order in synchronous with a clock signal, and each switching circuit 59 is switched ON by a signal from the shift register 57. Furthermore, each condenser 60 samples the level of the signal as data when each switching circuit 59 is turned ON, and when data in the same number as the number of the display cells in lateral direction are held in the condensers 60, the signal amplifier circuit 61 reads in data from the condensers 60 at one time. Then, the data is outputted over the data signal line S_j , thereby displaying a video signal on the display 53. In the above first image display device, the signal amplifier circuit 61 is selected among the first through tenth signal amplifier circuits.

In the first image display device, one of the first through tenth signal amplifier circuits is adopted as the signal amplifier circuit 61. Therefore, a voltage having the same level as the voltage held in a sampling-use condenser 60 can be sent over the data signal line S_j . As a result, the first image display device permits a high quality image display.

The second image display device having the arrangement of the first image display device is arranged such that the display cells and drive circuits 51 are formed on the same substrate.

The second image display device permits a compact size image display device in addition to

the effect of the first image display device.

The third image display device having the arrangement of the second image display device is arranged such that the substrate is composed of a transparent substrate having formed thereon a single crystal silicon thin film or polycrystalline silicon thin film formed on a transparent substrate.

In the third image display device, since the transparent substrate is used, a transmission type display device is enabled. Moreover, since an amorphous silicon thin film or a polycrystalline silicon thin film which permits a transistor having a high drive force is used, a practical drive circuit including a signal amplifier circuit can be manufactured. Especially when a transistor composed of a single crystal silicon thin film or polycrystalline silicon thin film is used, electric properties widely vary. However, with the above signal amplifier circuit, the variations can be adjusted.

The fourth image display device having the arrangement of the first, second or third image display device is arranged such that the level of the video signal is successive.

According to the fourth image display device, an image can be displayed with a successively varying gradation in addition to the effects of the first through third image display devices. Moreover, reversing of the gradation occurred when varying the gradation at every vertical line can be prevented.

The fifth image display device having the arrangement of the first, second or third image display device is arranged such that the video signal is discrete having at least four levels.

The fifth image display device offers the same effect of the fourth embodiment.

The sixth image display device having the arrangement of the first, second, third, fourth or fifth image display device is arranged such that each display cell includes a liquid crystal display element.

According to the arrangement of the sixth image display device, since each display cell includes the liquid crystal display element, in addition to the effects of the first through fifth image display devices, a display element having a uniform display characteristic can be obtained. Therefore, only by cancelling out the offset voltage ΔV generated in the buffer amplifier 1, a high quality image can be displayed.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A signal amplifier circuit comprising:
 - a buffer amplifier; and
 - adjusting means for detecting a difference in voltage as an offset voltage between a reference voltage and an output voltage from said buffer amplifier when the reference voltage is inputted thereto and for inputting a voltage obtained by subtracting the offset voltage from a voltage of an input signal into said buffer amplifier so as to cancel out the offset voltage.
2. The signal amplifier circuit as set forth in claim 1, wherein:
 - the input signal is inputted in synchronous with a clock, and the offset voltage is cancelled out every clock by said adjusting means.
3. The signal amplifier circuit as set forth in claim 1 or 2, wherein:
 - said adjusting means is composed of a first condenser and first through fifth switching elements;
 - an input terminal of said buffer amplifier is connected to an input terminal of the reference voltage through the first switching element and to one electrode of the first condenser through the second switching element;
 - said one electrode of the first condenser is connected to an input terminal of the input signal through the third switching element; and
 - the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to the input terminal of the reference voltage through the fifth switching element.
4. The signal amplifier circuit as set forth in claim 1 or 2, wherein:
 - said adjusting means is composed of first and second condensers and second through seventh switching elements;
 - an input terminal of said buffer amplifier is connected to one electrode of the first condenser through the second switching element and to a terminal of a constant voltage through the seventh switching element and the second condenser;
 - said one electrode of the first condenser is connected to an input terminal of an input signal through the third switching element and to an input terminal of the reference voltage through the sixth switching element; and
 - the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching
5. The signal amplifier circuit as set forth in claim 1 or 2, wherein:
 - said adjusting means is composed of first and third condensers and first, third, fourth and fifth switching elements;
 - an input terminal of said buffer amplifier is connected to an input terminal of the reference voltage through the first switching element and to one electrode of the first condenser;
 - said one electrode of said first condenser is connected to an input terminal of an input signal through the third switching element;
 - the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to an input terminal of the reference voltage through the fifth switching element; and
 - the other electrode of the first condenser is connected to a terminal of a constant voltage through the third condenser.
6. The signal amplifier circuit as set forth in claim 1, 2, 3, 4 or 5, wherein:
 - an eighth switching element for applying the reference voltage to an output from said buffer amplifier is provided.
7. The signal amplifier circuit as set forth in claim 1, 2, 3, 4 or 5, wherein:
 - a ninth switching element for separating said buffer amplifier from an external load is provided.
8. The signal amplifier circuit as set forth in claim 3, 4 or 5, wherein:
 - at least one of the switching elements is a complementary MOS transistor switch.
9. An image display device comprising:
 - a display composed of display cells arranged so as to form a matrix;
 - a first drive circuit for sampling a video signal so as to send a voltage obtained as data by sampling over a data signal line; and
 - a second drive circuit for selecting a scanning signal line in order so as to send data on the data signal line to each display cell,
 - wherein said first drive circuit includes:
 - a shift register;
 - switching circuits in the same number as the number of display cells in a lateral direction;
 - sampling-use condensers in the same

number as the number of said switching circuits; and

signal amplifier circuits in the same number as the number of said sampling-use condensers,

said shift register sends a signal in order into each switching circuit synchronous with a clock signal,

the switching circuit is then set ON when receiving a signal from said shift register,

each sampling-use condenser samples a level of a video signal obtained as data when the switching circuit is set ON,

when data in the same number as the number of the display cells in a lateral direction are held in said sampling-use condensers, said signal amplifier circuits take-in the data from said sampling-use condensers at one time and output the data over the data signal line, thereby displaying the video signal on said display, and

said signal amplifier circuit includes:

a buffer amplifier; and

adjusting means for detecting a difference in voltage as an offset voltage between a reference voltage and an output voltage from said buffer amplifier when the reference voltage is inputted thereto, and for inputting a voltage obtained by subtracting the offset voltage from a voltage of a video signal sampled by each sampling-use condenser into said buffer amplifier so as to cancel out the offset voltage.

10. The image display device as set forth in claim 9, wherein:

the offset voltage is cancelled out by said adjusting means every clock.

11. The image display device as set forth in claim 10, wherein:

said adjusting means is composed of a first condenser and first through fifth switching elements;

an input terminal of said buffer amplifier is connected to an input terminal of the reference voltage through the first switching element and to one electrode of the first condenser through the second switching element;

said one electrode of the first condenser is connected to an input terminal of an input signal through the third switching element; and

the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to the input terminal of the reference voltage through the fifth switching element.

12. The image display device as set forth in claim 10, wherein:

said adjusting means is composed of first and second condensers and second through seventh switching elements;

an input terminal of said buffer amplifier is connected to one electrode of the first condenser through the second switching element and to a terminal of a constant voltage through the seventh switching element and the second condenser,

said one electrode of the first condenser is connected to an input terminal of an input signal through the third switching element and to an input terminal of an reference voltage through the sixth switching element, and

the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to the input terminal of the reference voltage through the fifth switching element.

13. The image display device as set forth in claim 10, wherein:

said adjusting means is composed of first and third condensers and first, third, fourth and fifth switching elements;

an input terminal of said buffer amplifier is connected to an input terminal of a reference voltage through the first switching element and to one electrode of the first condenser;

said one electrode of said first condenser is connected to an input terminal of an input signal through the third switching element;

the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to the input terminal of the reference voltage through the fifth switching element; and

the other electrode of the first condenser is also connected to a terminal of a constant voltage through the third condenser.

14. The image display device as set forth in claim 9, 10, 11, 12 or 13 wherein:

an eighth switching element for applying the reference voltage to an output from said buffer amplifier is provided.

15. The image display device as set forth in claim 9, 10, 11, 12 or 13 wherein:

a ninth switching element for separating said buffer amplifier from an external load is provided.

16. The image display device as set forth in claim 11, 12 or 13 wherein:
at least one of the switching elements is a complementary MOS transistor switch. 5
17. The image display device as set forth in claim 9, wherein:
said display cells and said first drive circuit are formed on the same substrate. 10
18. The image display device as set forth in claim 17, wherein said substrate comprises:
a transparent substrate having formed thereon an amorphous silicon thin film or polycrystalline silicon thin film. 15
19. The image display device as set forth in claim 9, 17 or 18, wherein:
a level of the video signal is consecutive. 20
20. The image display device as set forth in claim 9, 17 or 18, wherein:
the video signal is discrete having at least four levels. 25
21. The image display device as set forth in claim 9, 17, 18, 19, 20, 21 or 22, wherein:
each display cell includes a liquid crystal display element. 30
22. The signal amplifier circuit as set forth in claim 1, wherein said adjusting means includes:
a first condenser; and
switching means which applies an output voltage from said buffer amplifier when a reference voltage is inputted thereto to a first electrode of a condenser and applying a voltage of an input signal to a second electrode of the condenser, and thereafter, applies the reference voltage to the first electrode of the condenser and connects the second electrode to said buffer amplifier. 35 40

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50

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FIG.1

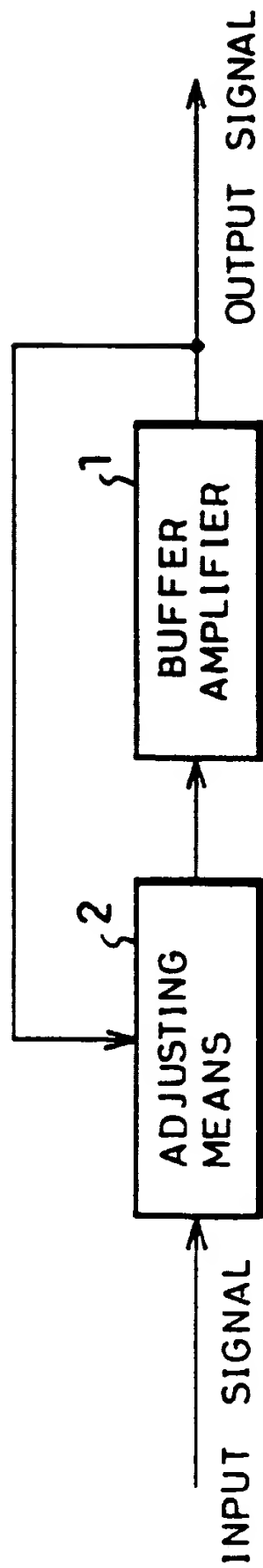


FIG. 2

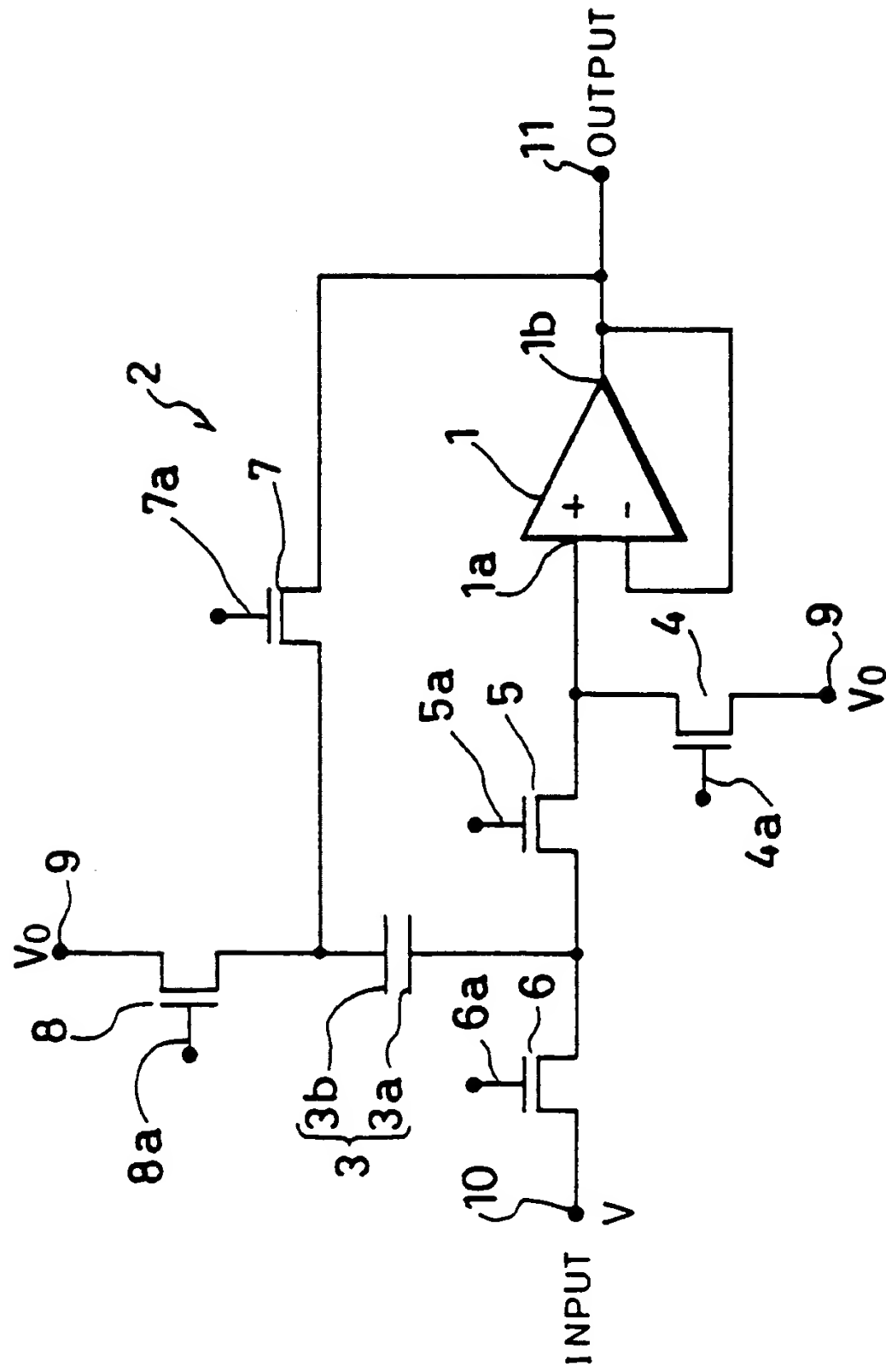


FIG. 3

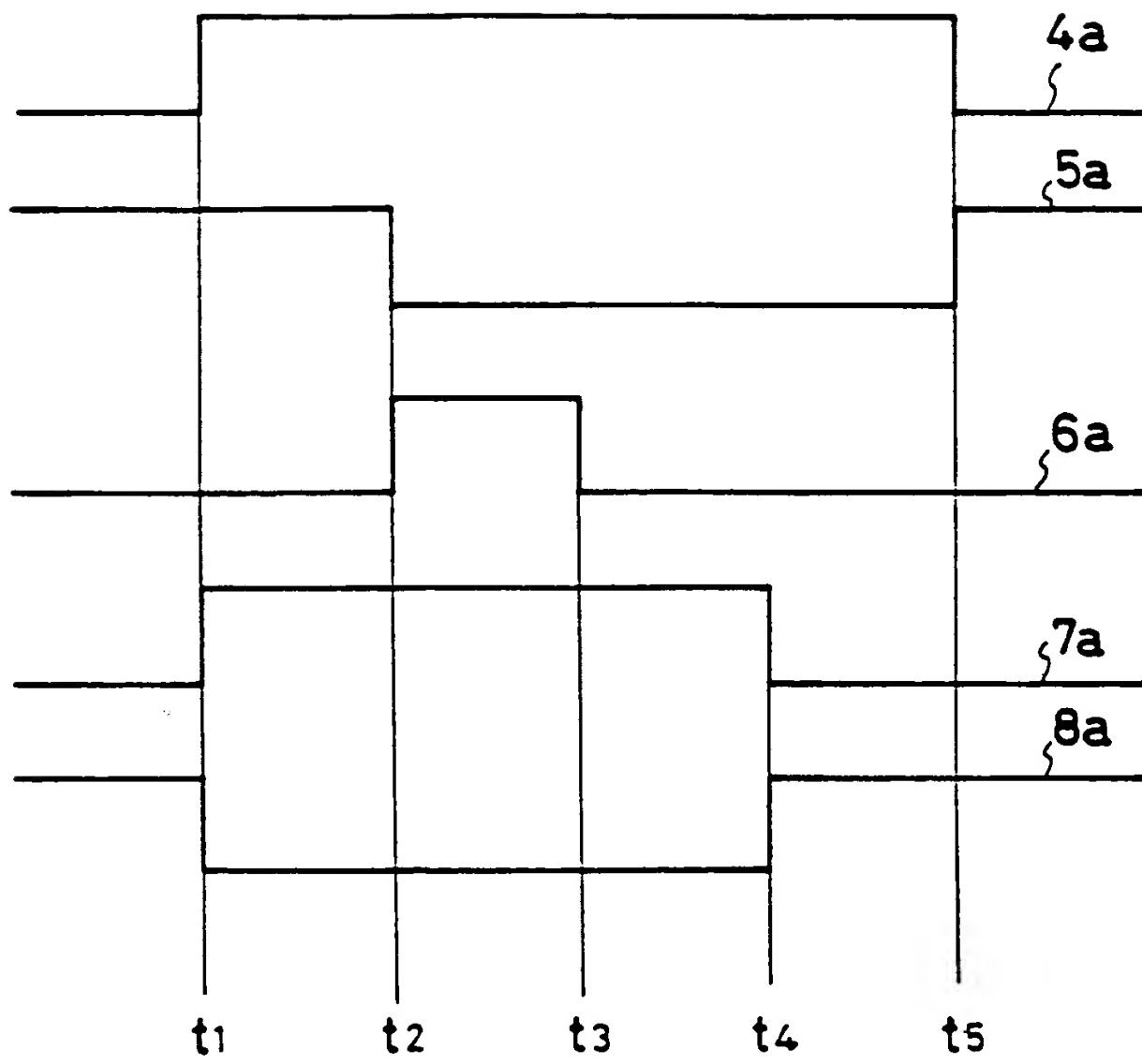


FIG. 4

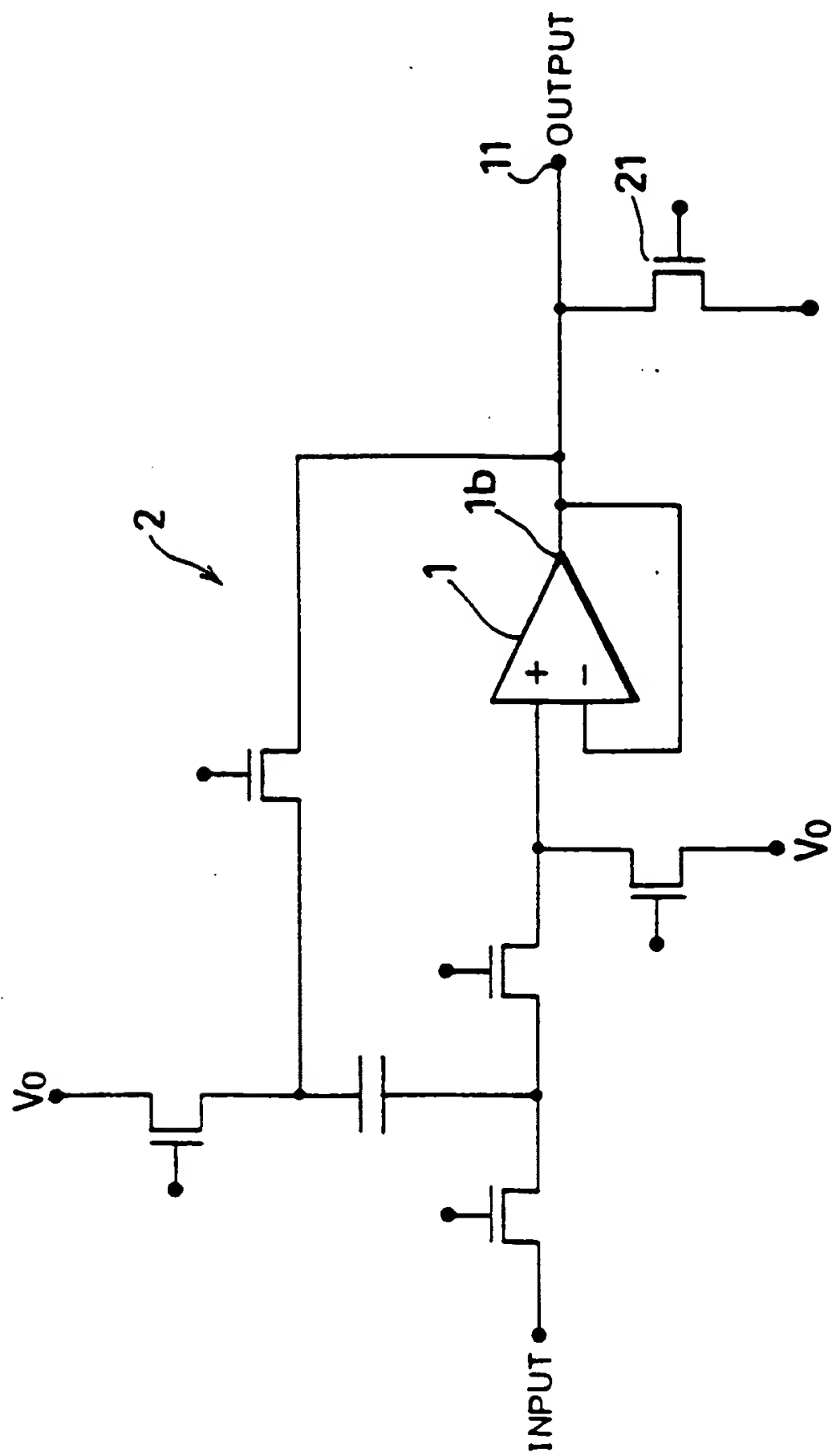


FIG. 5

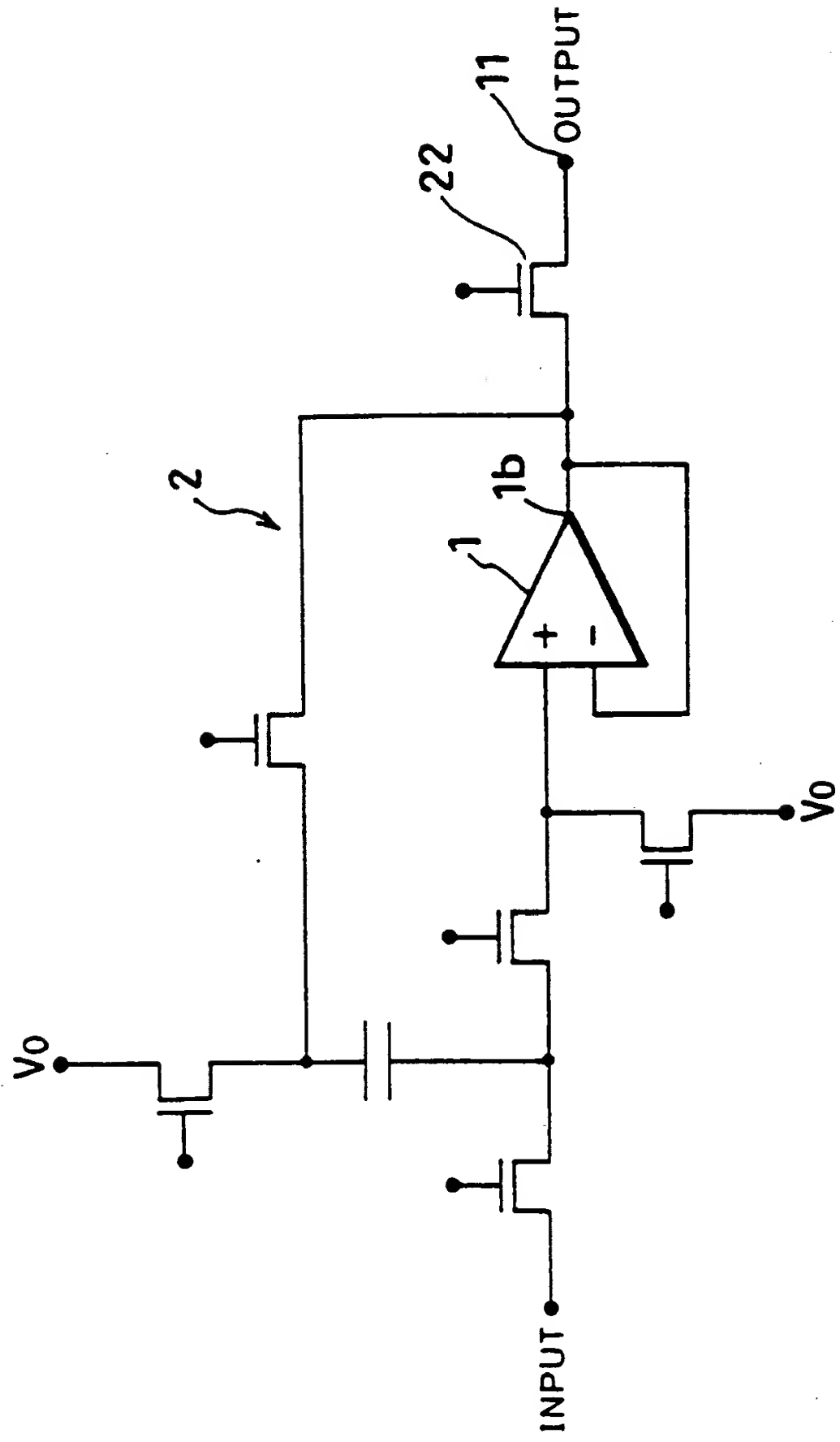


FIG. 6

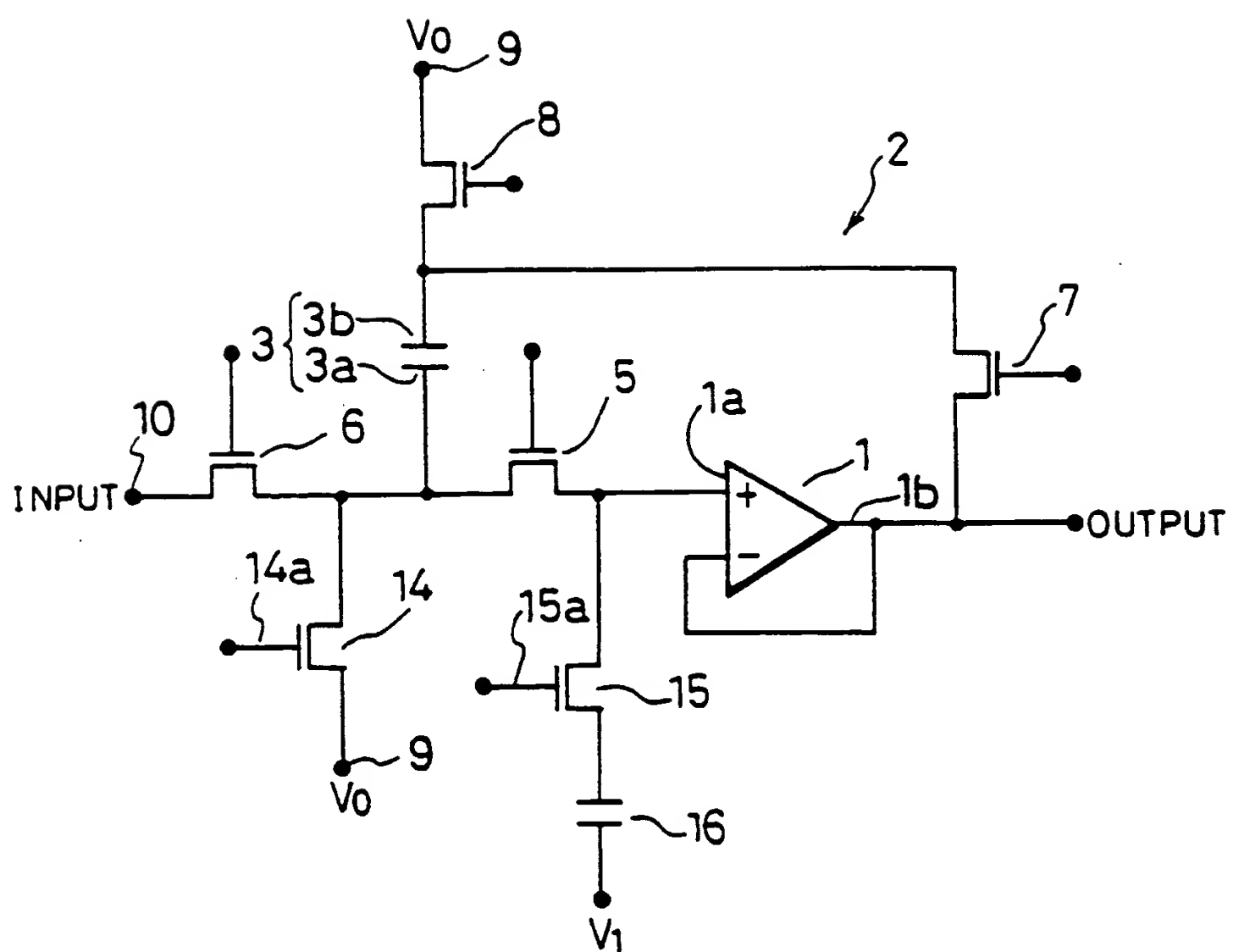


FIG. 7

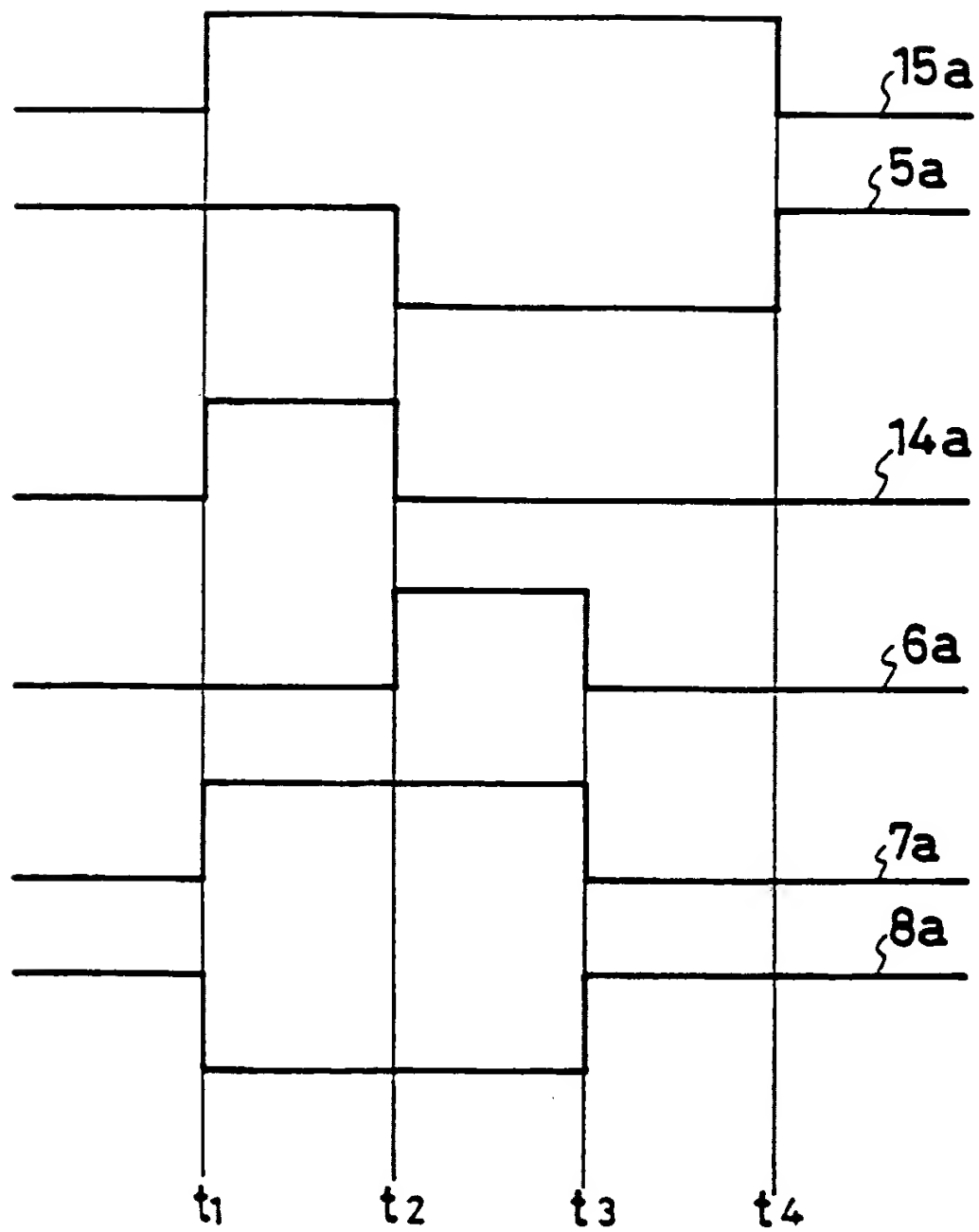


FIG. 8

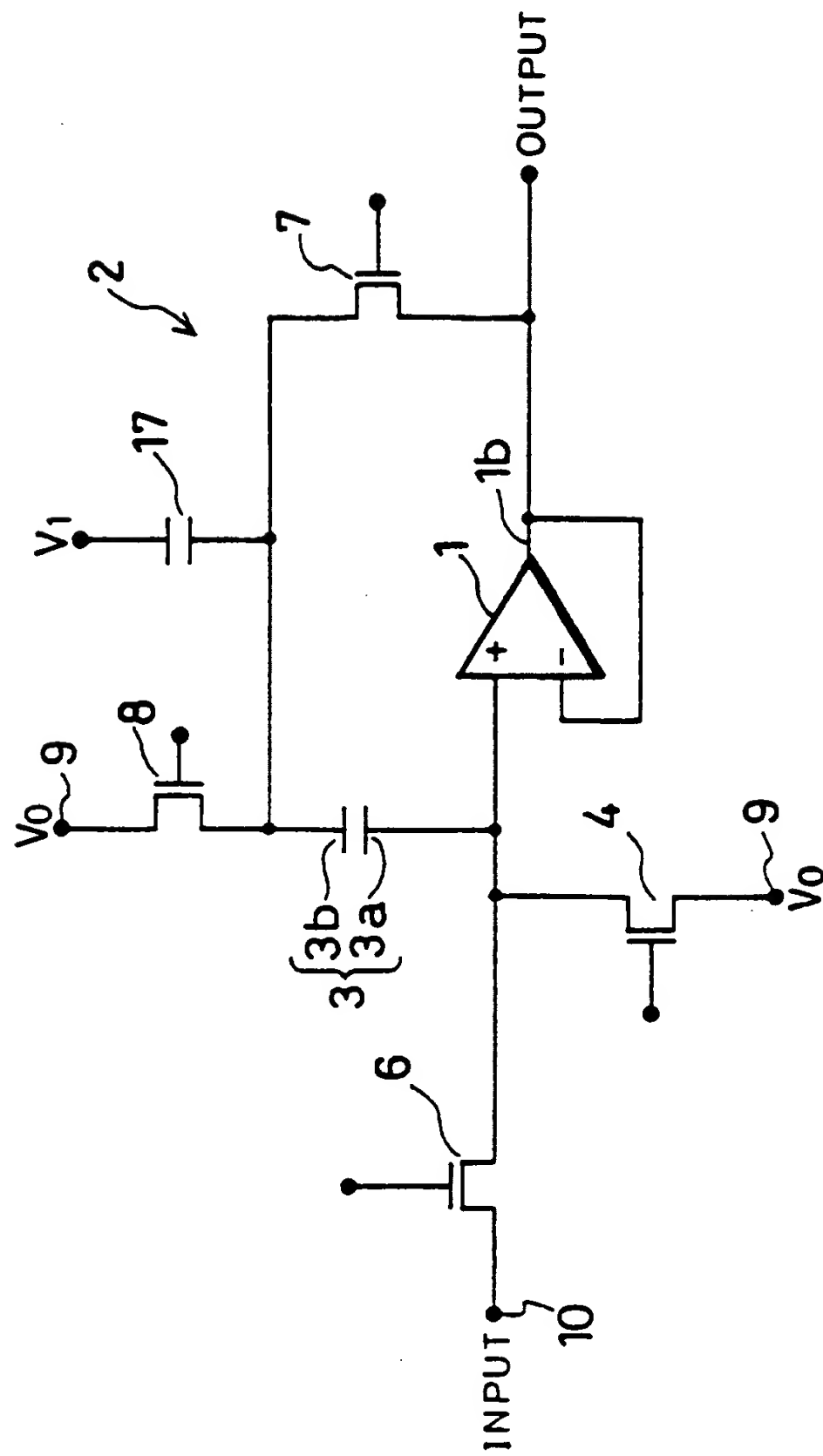


FIG. 9

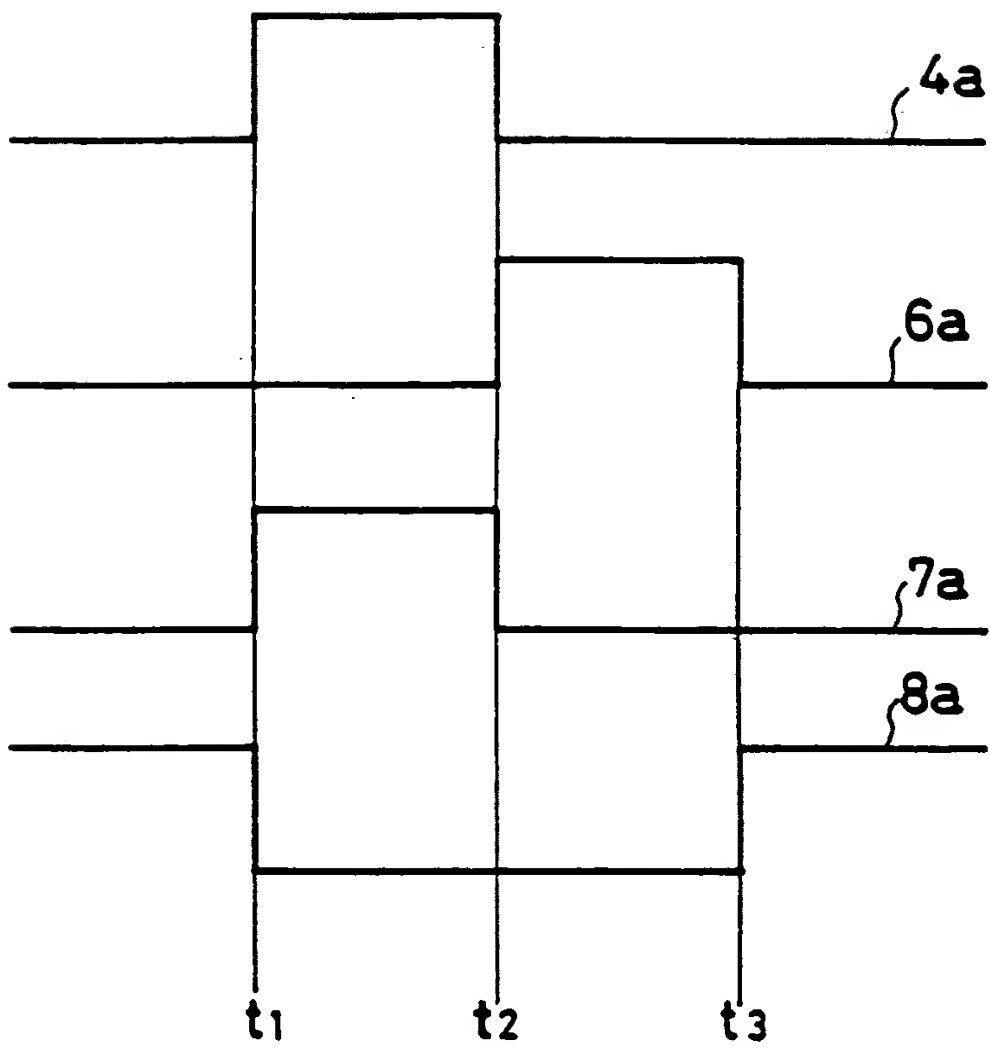


FIG.10

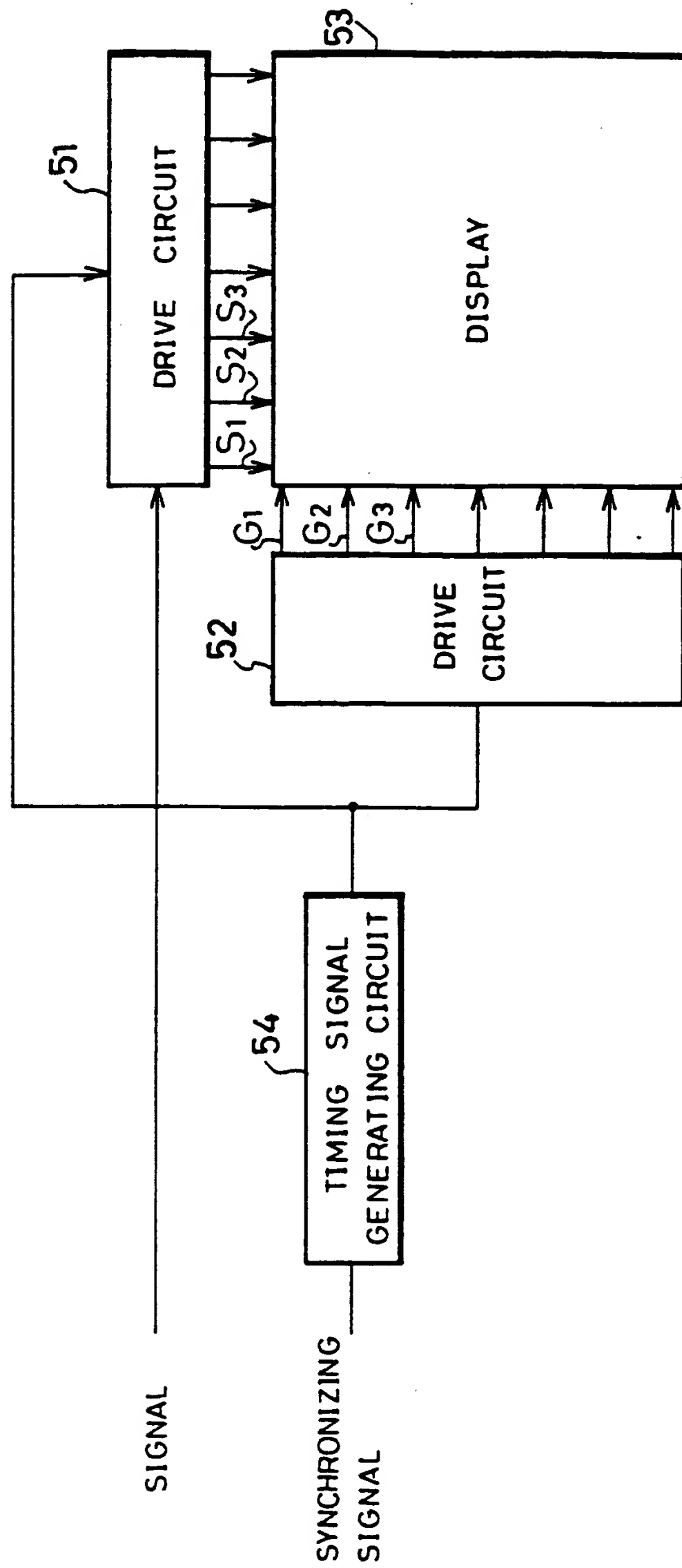
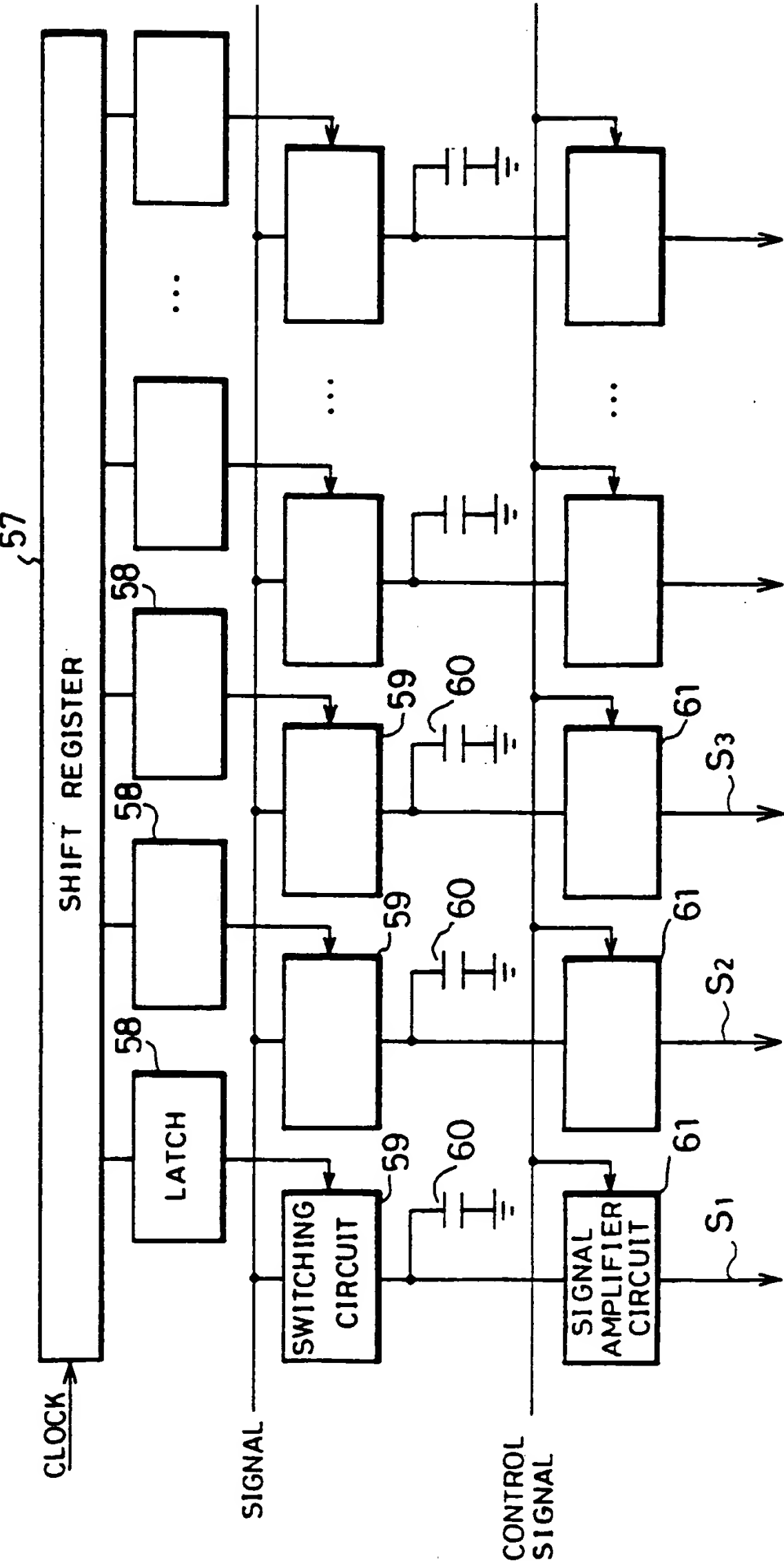


FIG. 11



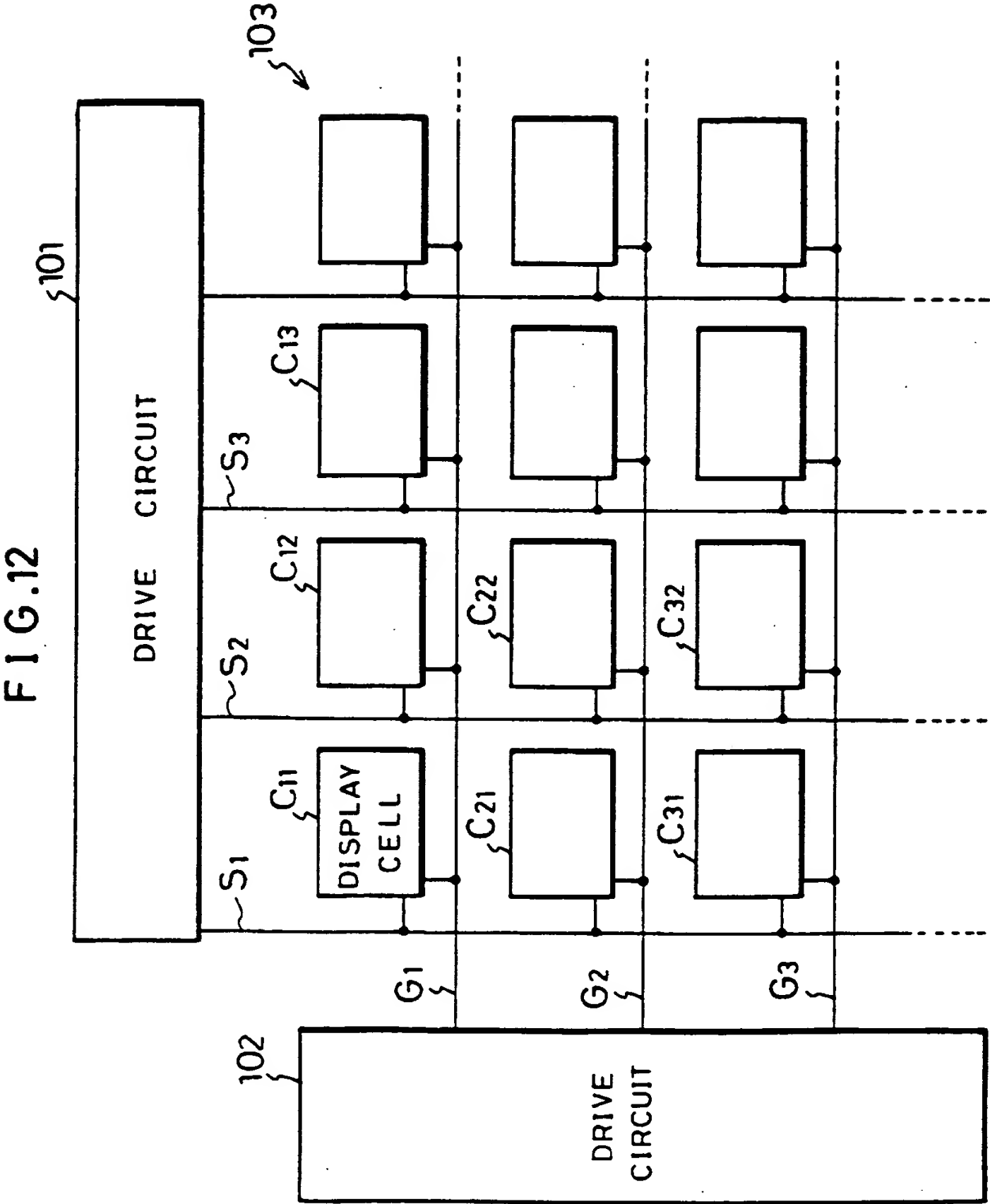


FIG. 13

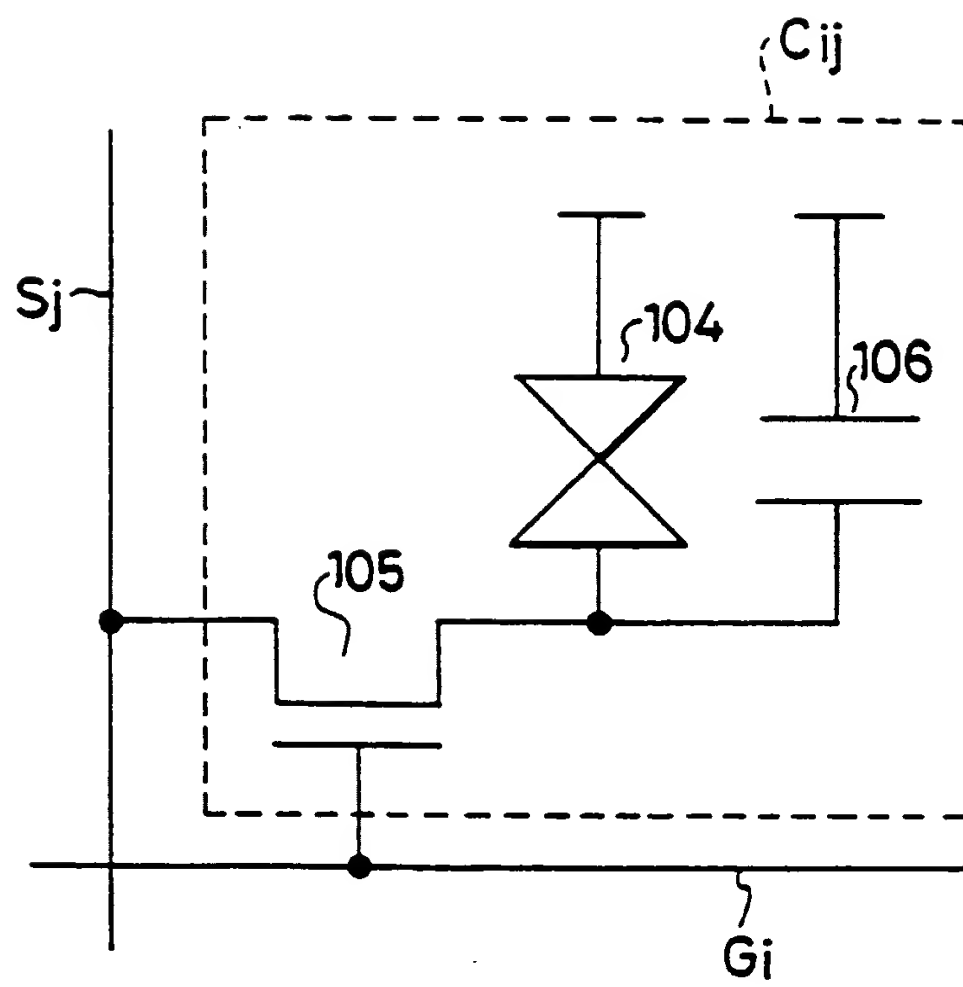


FIG. 14

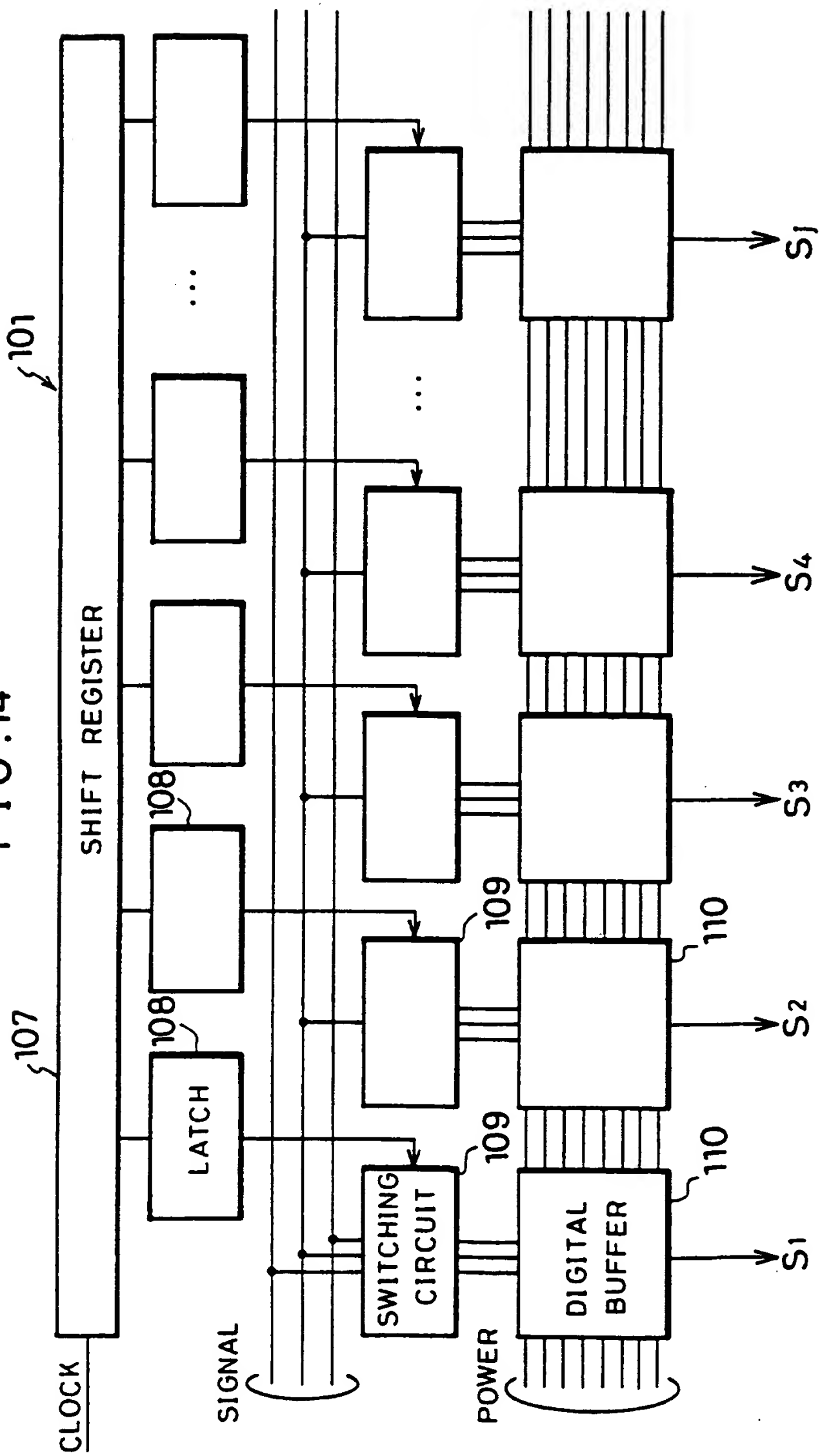


FIG. 15

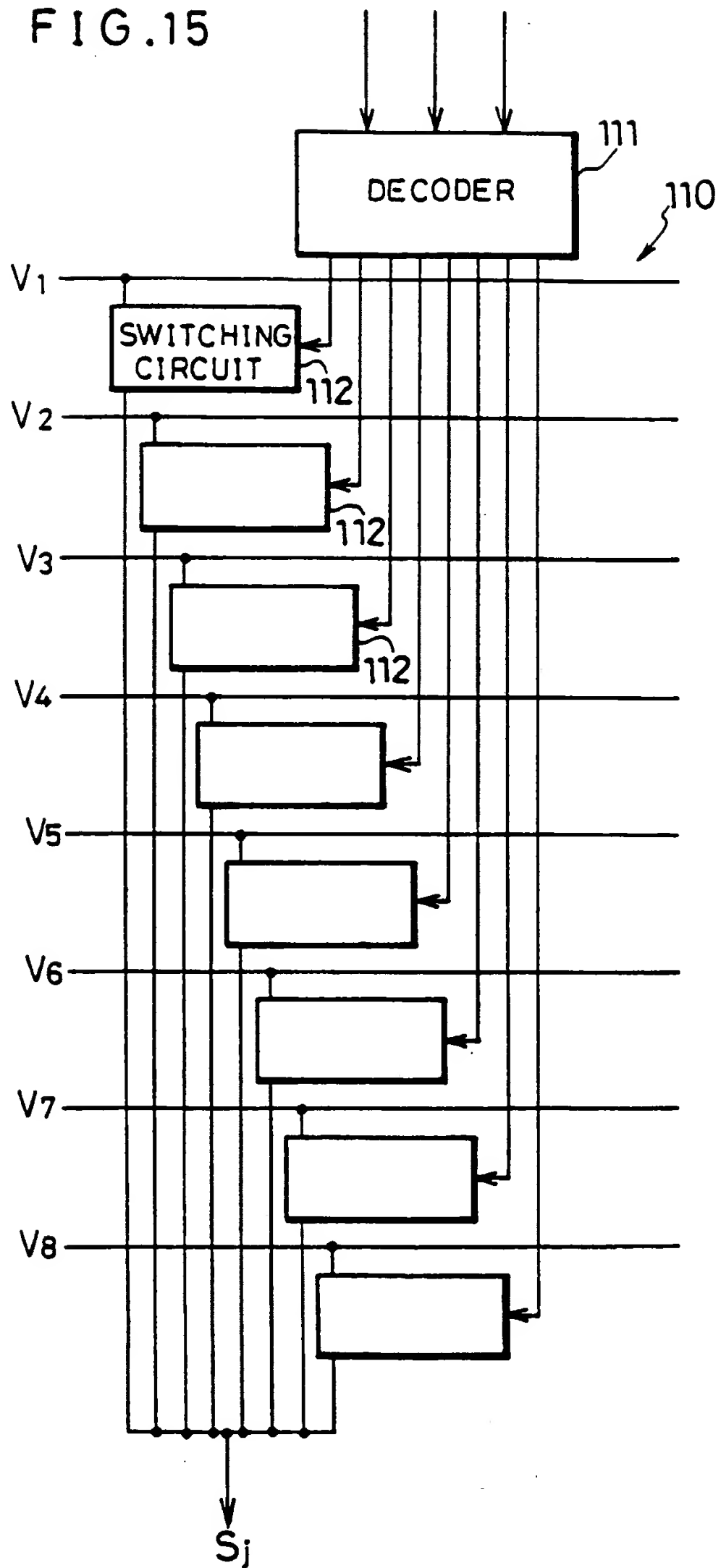


FIG. 16

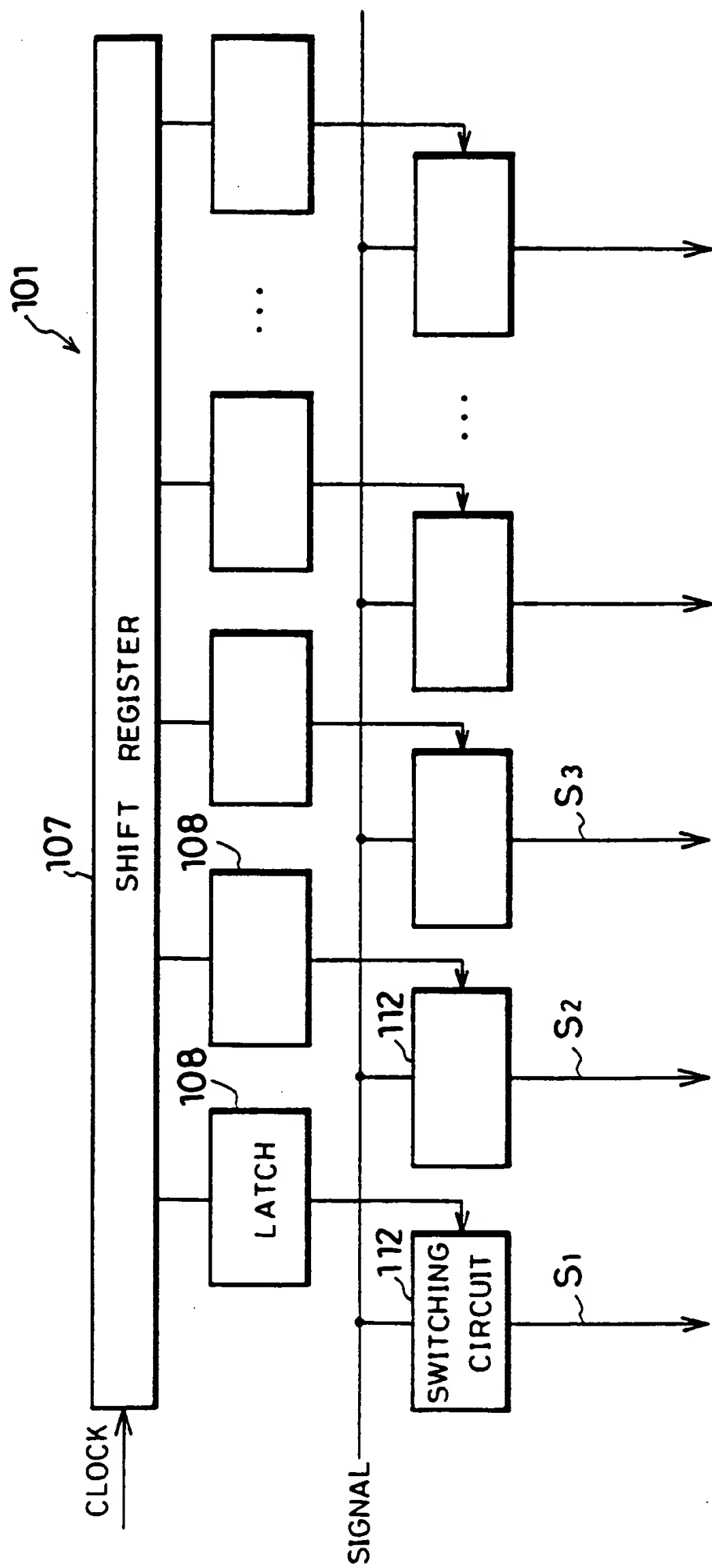


FIG. 17

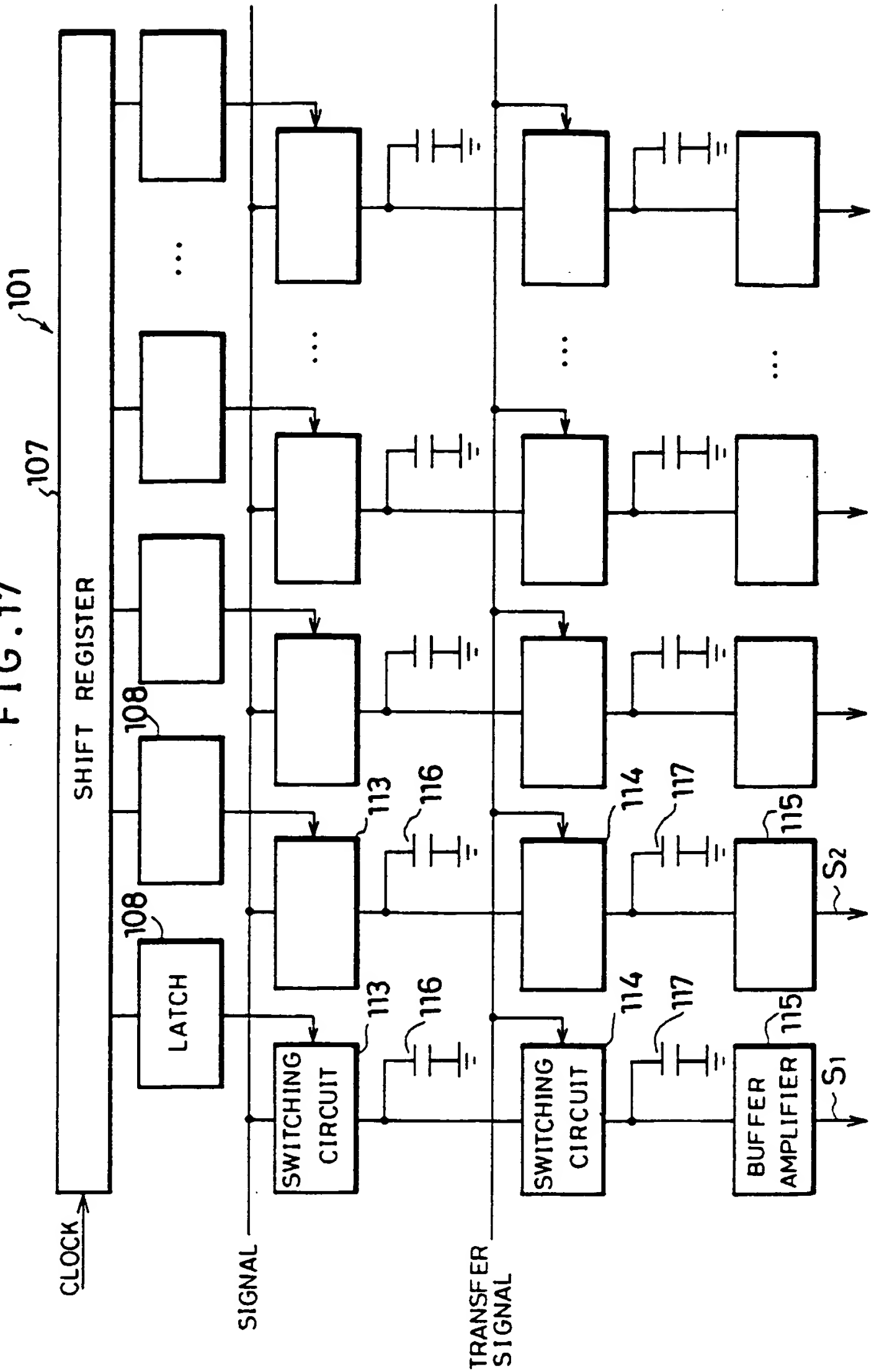


FIG. 18

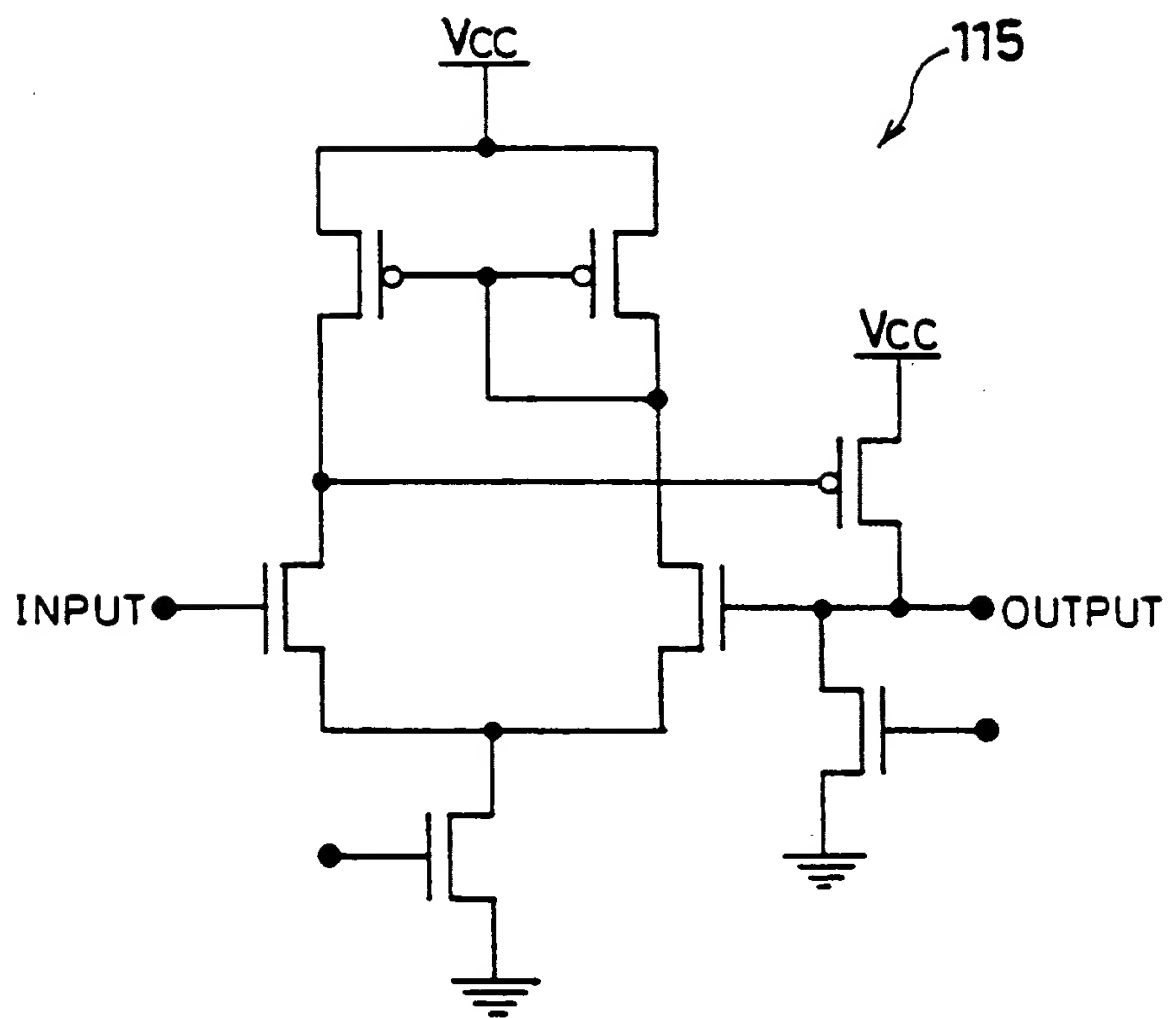


FIG. 19

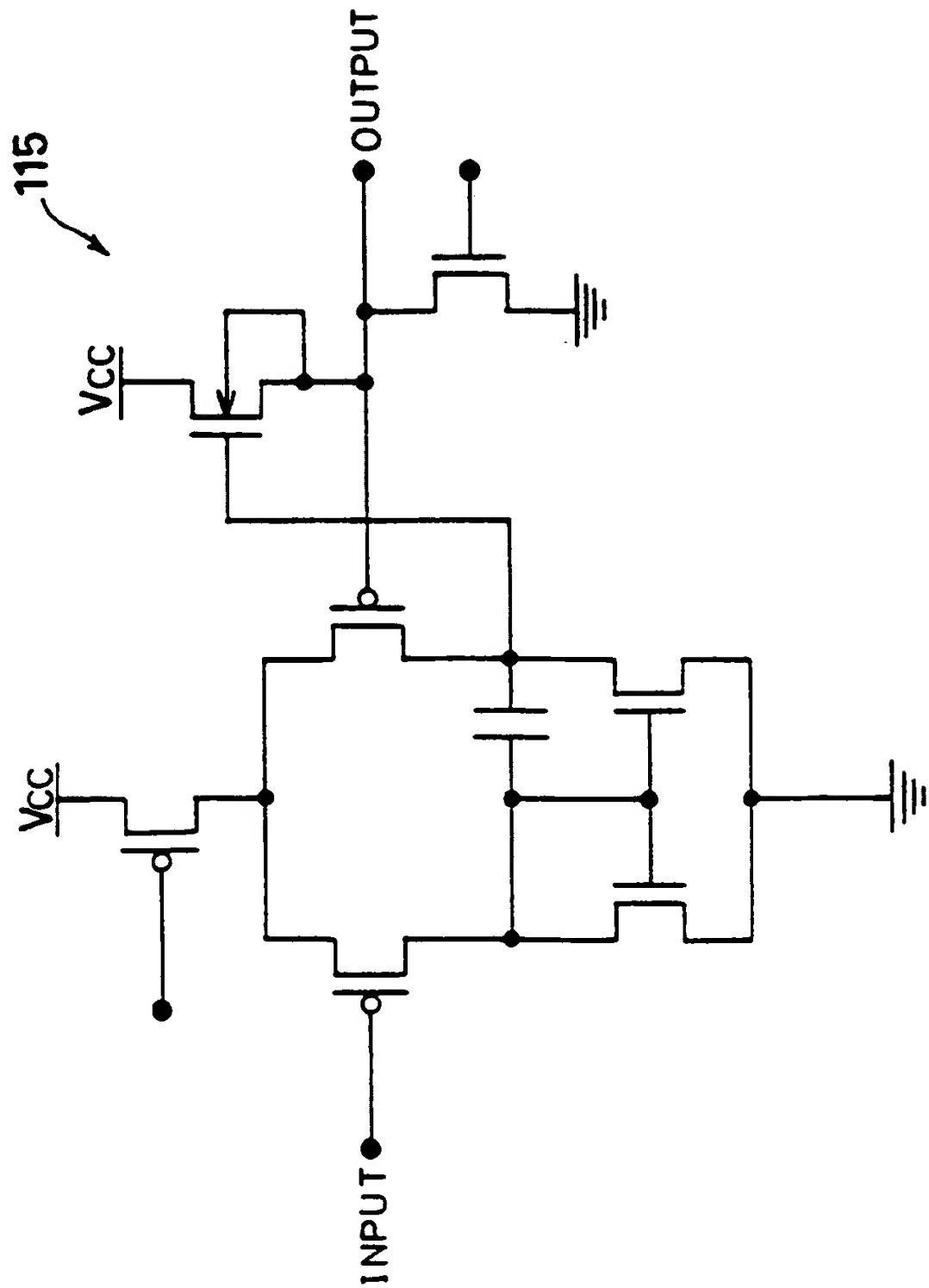


FIG. 20

